New Beam Loss Monitor for 12 GeV Upgrade*

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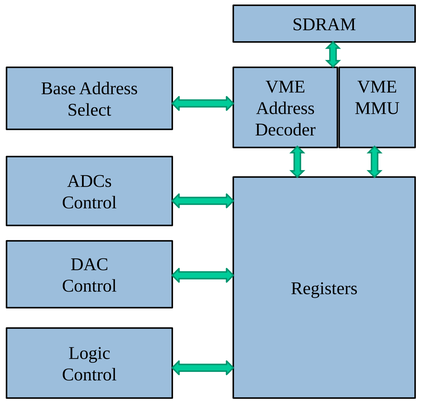
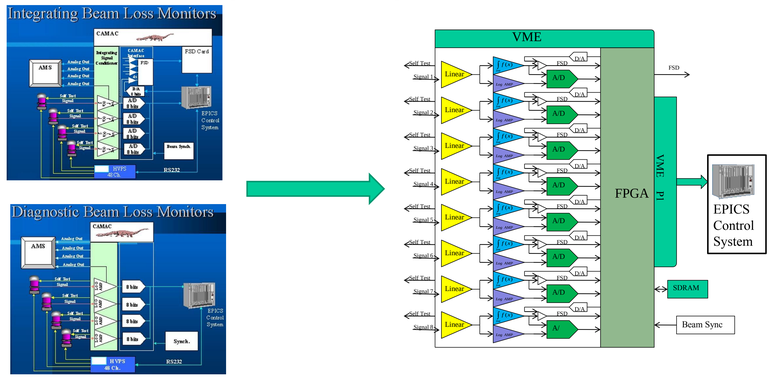
Abstract

This paper describes a new VME based machine protection Beam Loss Monitor(BLM) signal processing board designed at Jefferson Lab to replace current CAMAC based BLM board. The new eight-channel BLM signal processor has linear, logarithmic, and integrating amplifiers that simultaneously provide the optimal signal processing for each application. Amplified signals are digitized and then further processed through a Field Programmable Gate Array (FPGA). Combining both the diagnostic and machine protection functions in each channel allows the operator to tune-up and monitor beam operations while the machine protection is integrating the same signal. Other features include extensive built-in-self-test, fast shutdown interface (FSD), and 16-Mbit buffers for beam loss transient play-back. The new VME BLM board features high sensitivity, high resolution, and low cost per channel.

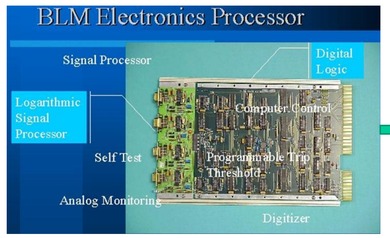
FPGA Program Function Modules



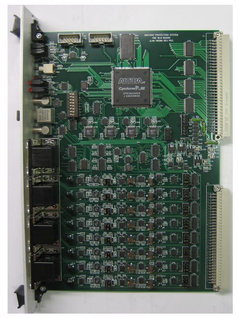
BLM Signal Processing Board Upgrade



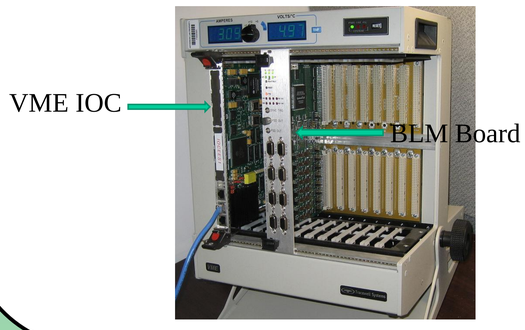
CAMAC BLM Board



New VME BLM Board



New BLM Board in VME Crate



New BLM Attributes

- Provide both machine protection and diagnostic functions.
- Instantaneous readback of beam loss.
- 16 bit digital output for integrating signal and logarithmic signal.
- Fast response, << 1 us response time for integrating, 10nA^2 for log.
- Wide dynamic range (> 50 dB) for logarithmic signal.
- Built-in self test and onboard signal injection.
- FPGA controlled.
- Local data buffer for integrating and logarithmic signal.
- VME interface and fully integrated into EPICS.
- Pulse beam measurement and continuous monitoring.
- Low cost ($100 per sensors).

Conclusions

The prototype of a new VME based BLM signal processing board is developed to upgrade the existing CAMAC board. The board provides both diagnostic and machine protection functions. Each board controls 8 PMT sensors to dramatically cut the cost per sensors. The software for the FPGA programming and EPICS are under developed. Further test and debug of the BLM board are planning to execute. The test with PMT and FSD system on the accelerator operation environment is required. The new design will provide a low cost BLM solution for the CEBAF 12 GeV upgrade.

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