WEP039: Timing System Upgrade for SNS

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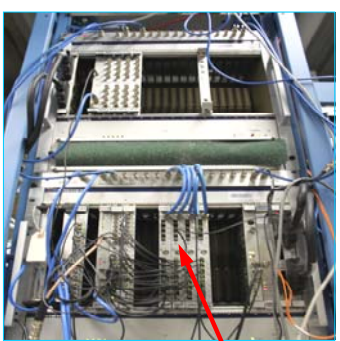
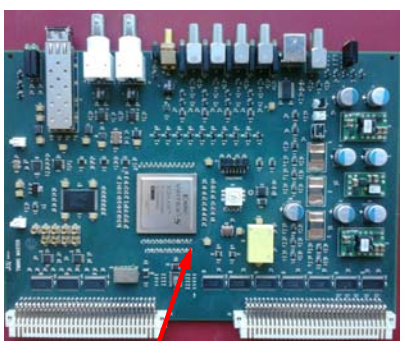
Abstract

A timing system is a crucial subsystem of every accelerator, responsible for orchestrating the entire machine cycle by cycle. The current SNS timing system is based on the modified BNL solution which in turn is based on previous systems at other sites. The timing master is a collection of low functionality VME building blocks that are highly dependent on creative software to achieve the needed system functionality. The implementation technology of the whole system is backdated, making it impossible to build and maintain spares and boards for machine upgrades. At SNS we chose a roadmap which would allow a gradual upgrade of the timing system without having to redesign everything at once and yet provide a path for future modernization of the infrastructure. This paper presents progress on new timing master and receiver card, which will provide us with more flexible control and greater reliability by tremendously reducing the component count while still retaining compatibility with existing timing receiver units. The designs emphasize the use of FPGA technology in a way that simplifies the supporting software. The design of the system is a collaboration effort of ORNL and Cosylab.

A New Timing Master

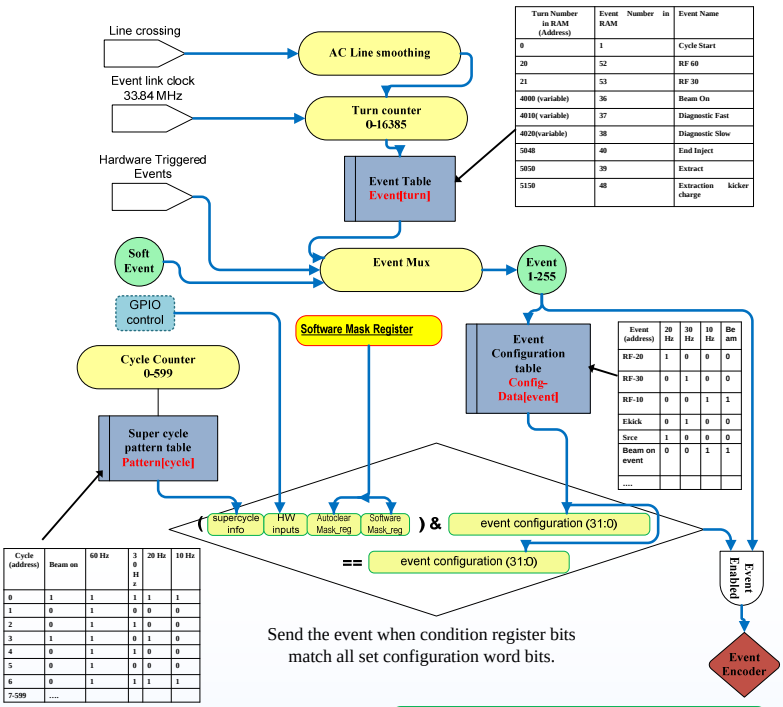




Feature	Old	New
Generation of fixed events	Gate cards triggering an event encoder. Events constantly have to be re-timed. Not expandable without adding hardware.	Table driven with a memory location corresponding to a position in the event link time line.
Event collision control	Protects cycle start but not the extract event. MPS events jostle fixed events.	Only one event for every 16 bit clock times. Fixed events are selected first.
Super Cycle Pattern (Run time)	Generation of non 60 Hz events require participation by software	Implemented entirely in hardware.
RTDL Generator	Spans multiple cards, needs pre-loaded map table, not expandable without adding hardware	Single memory mapped array that includes per frame enable bits.
Generation of RTDL Data	All done in software including message CRC.	Hardware maintains time stamp and other critical RTDL data even when the software is not running.
System Hardware Requirements	1 CPU board, 1 Event encoder using 3 boards, 4 timing delay gates, 1 RTDL encoder using 5 boards, a GPS board, a frequency counter, a fan out module, a utility module, and a set of bus extenders for two VME crates.	1 CPU Board, 1 timing master board, and one GPS board.

The SNS is working toward a 95% beam availability goal during scheduled operation. Historically, timing master outages have been software related and no different than any other IOC. By keeping the machine running without software help, timing master outages are limited to minutes not hours.

Hardware Pattern Generator



Turn Number in RAM (Address)	Event Number in RAM	Event Name
0	1	Cycle Start
20	52	RF 60
21	53	RF 30
4000 (variable)	36	Beam On
4010(variable)	37	Diagnostic Fast
4020(variable)	38	Diagnostic Slow
5048	40	End Inject
5050	39	Extract
5150	48	Extraction kicker charge

Event (address)	20 Hz	30 Hz	10 Hz	Beam
RF-20	1	0	0	0
RF-30	0	1	0	0
RF-10	0	0	1	1
Ekick	0	1	0	0
Scrc	1	0	0	0
Beam on event	0	0	1	1
....				

Cycle (address)	Beam on	60 Hz	30 Hz	20 Hz	10 Hz
0	1	1	1	1	1
1	0	1	0	0	0
2	0	1	1	0	0
3	1	1	0	1	0
4	0	1	1	0	0
5	0	1	0	0	0
6	0	1	1	1	1
7-599	....				

AUTO RTDL FRAMES

A few SNS RTDL frames are needed at all times. The hardware provides them when the IOC is down.

RTDL overwrite values:

- 001 – time stamp / secs(31:8)
  // HW generated timestamp
- 002 – time stamp / nsecs(7:0) + status(7:0) + secs(7:0)
  // HW generated timestamp + mid-frame status
- 003 – time stamp / nsecs(31:8)
  // HW generated timestamp
- 004 – HW measured ring revolution period
  // based on measured clock period
- 015, 017, 035 – 0x00000000
  // Includes beam flavor
- 024 – VETO_NO_BEAM
- 025 – super-cycle number

A New Timing Receiver

Schematic development is under way at ORNL. The FPGA code design will leverage several existing designs. For the event link clock data recovery function an ADN 2816 chip is a proven performer. After testing prototypes we will build 25 modules for installation in selected locations. Phase in of this receiver will occur as replacements and installations are needed.