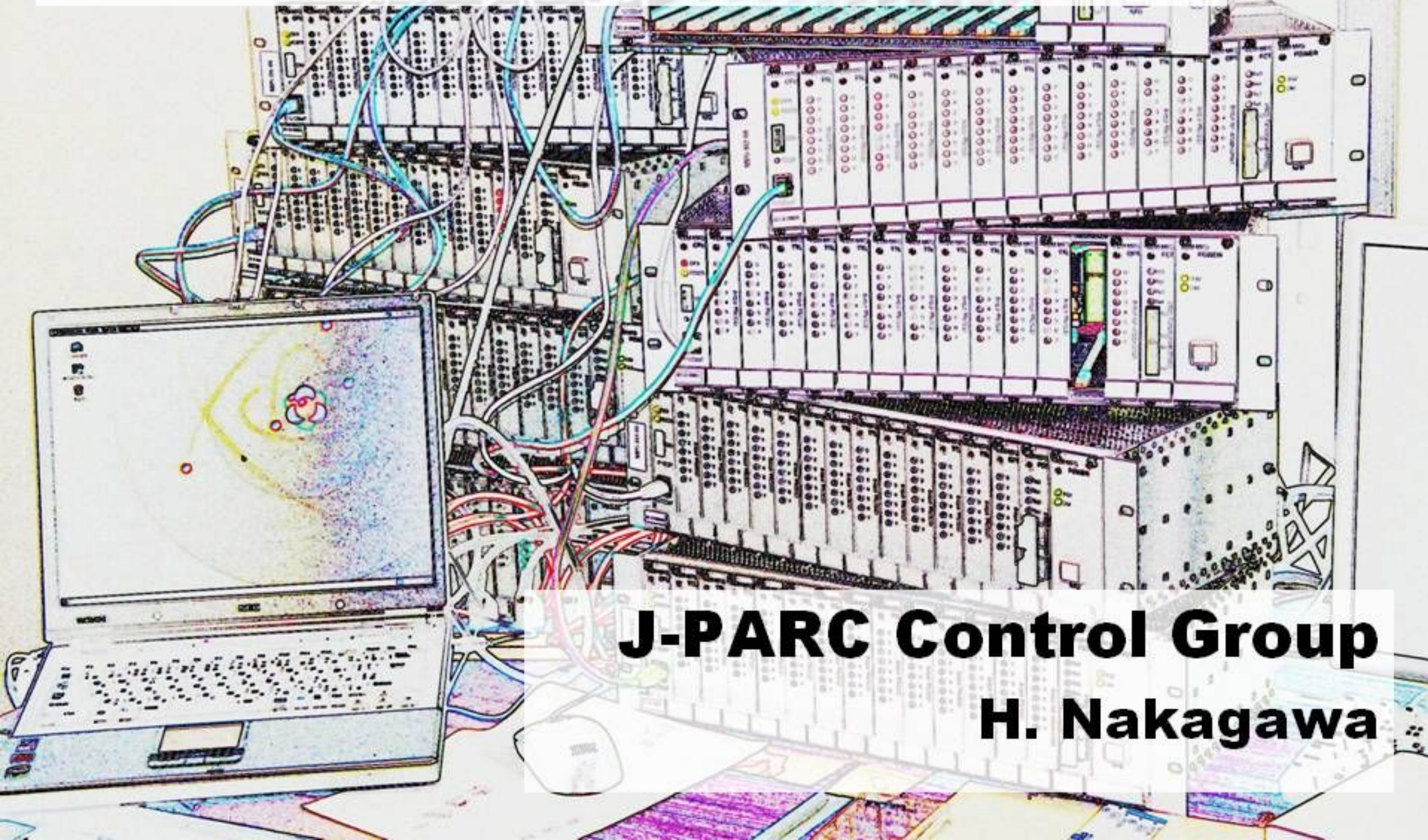


The Accelerator Protection System Based on Embedded EPICS for J-PARC

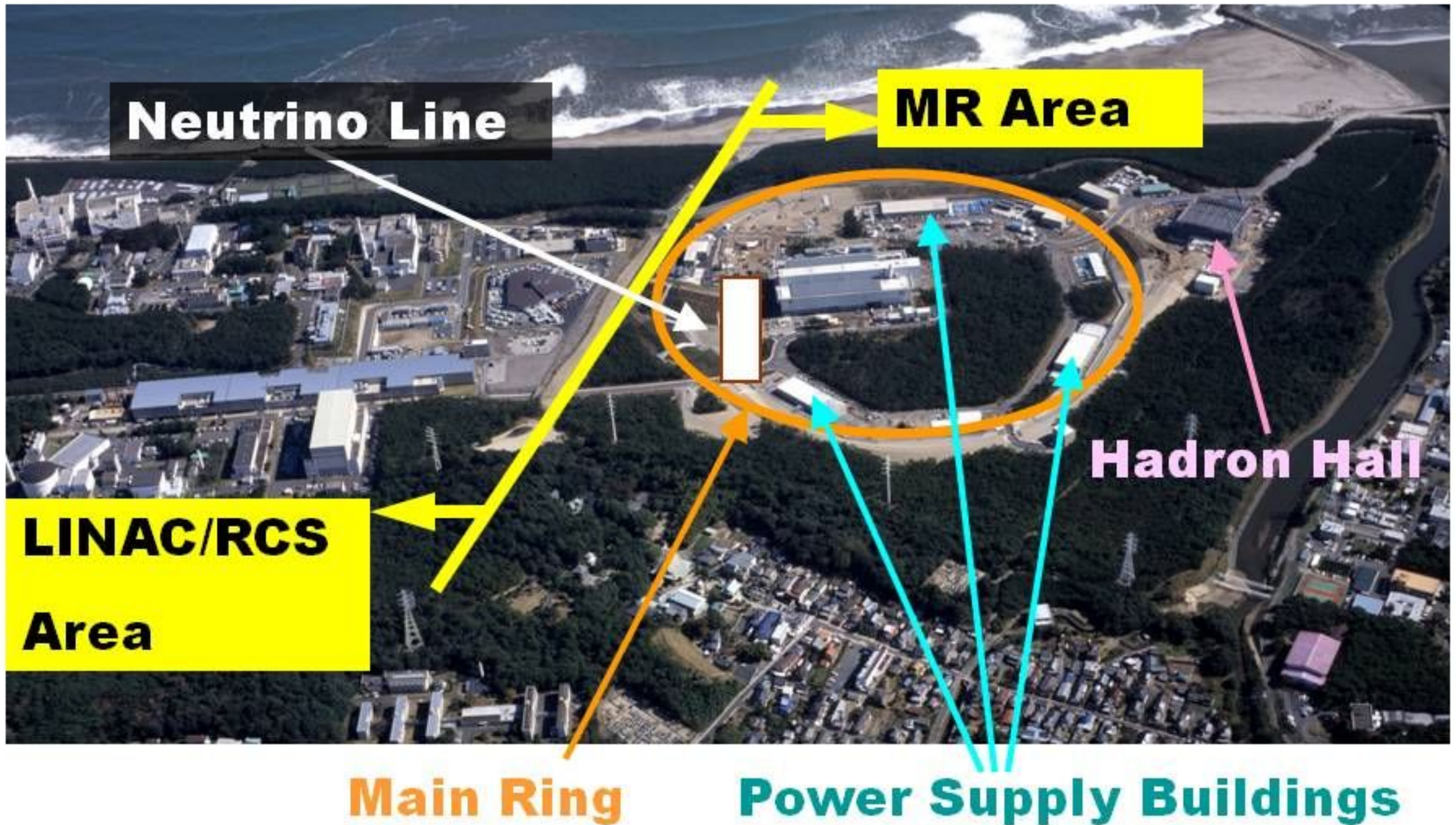


J-PARC Control Group
H. Nakagawa

Contents

- **J-PARC MR**
- **MR MPS design**
- **MR MPS modules**
- **Signal Handling for Quick Response and Maintainability**
- **Operational Results**
- **Summary**

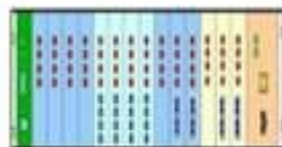
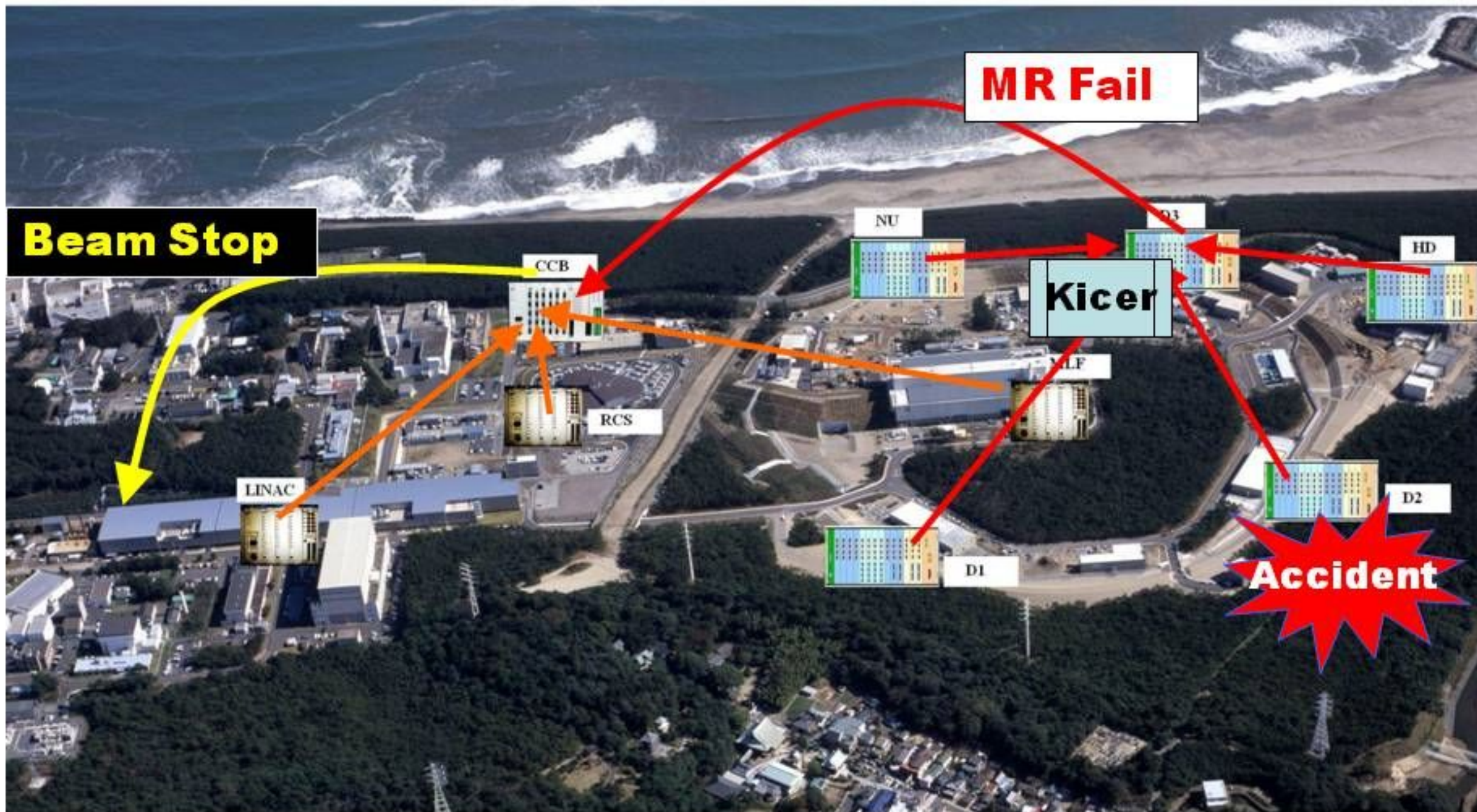
MR area of J-PARC



Goal of MPS(MR)

- **MR Design Guidelines**
 - **Response Time (<10us)**
 - **Flexibility of the Logic**
 - **Flexibility of the System**
 - **High Reliability**
 - **Maintainability**

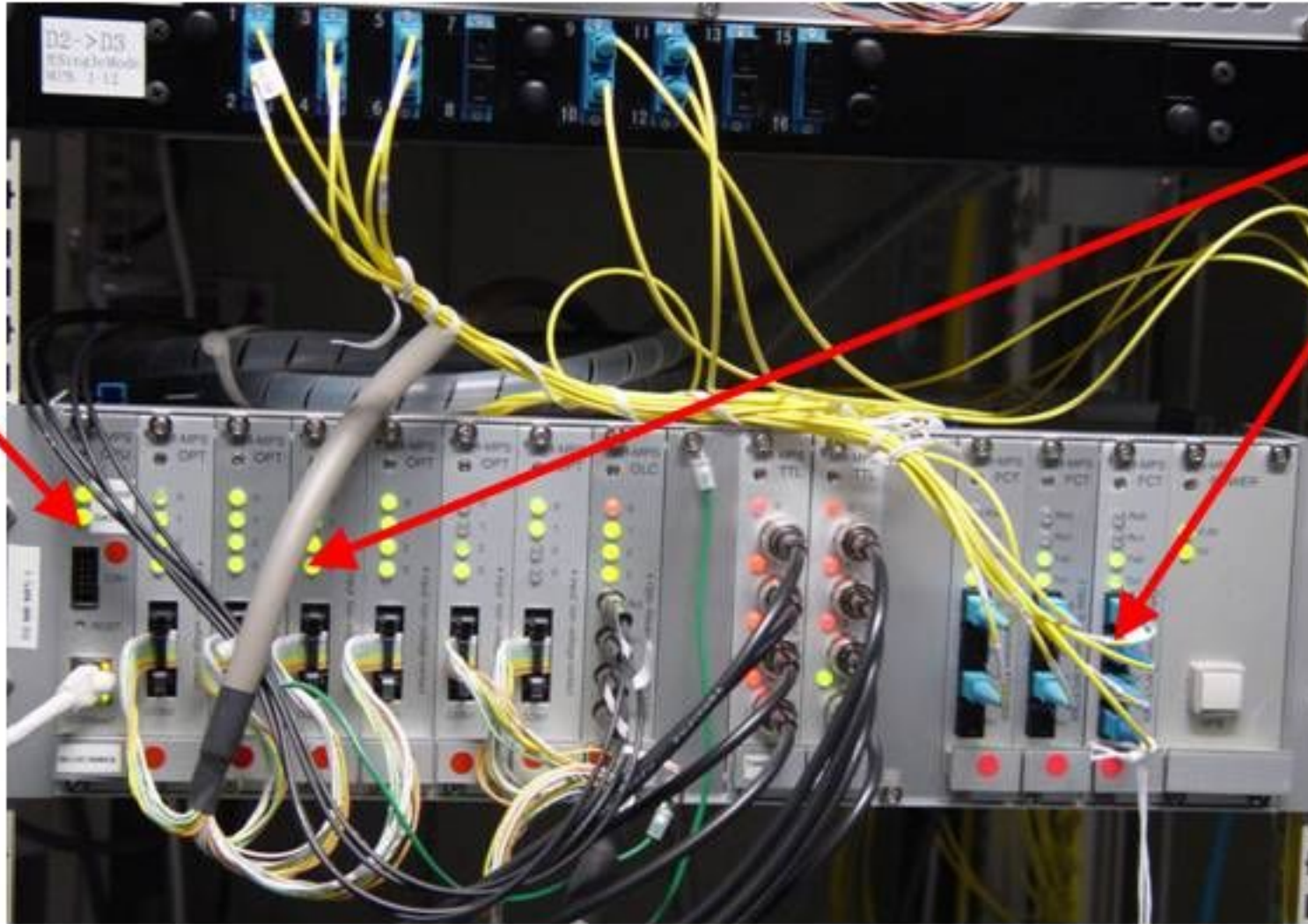
System Configuration



= Subrack for MR MPS

An MPS Subrack

CPU



IO modules

Link modules



MR MPS Modules

Category	Function	Name	ID Code
MR-MPS/Abort	Backplane	MR-MPS-BUS	
	Contact Signal Input	MR-MPS-OPT	2
	Optically Isolated Input	MR-MPS-OLC	3
	TTL Input	MR-MPS-TTL	4
	Long-Distance Optical Transceiver	MR-MPS-FCT	1
	TTL/Contact Input	MR-MPS-GIO (TTL/Contact)	5 / 6
	CPU(IOC)	MR-MPS-CPU	
	Power Supply	MR-MPS-POWER	
MR Beam Loss	Backplane	BLM-MPS-BUS	
	TTL Input(8 channels)	BLM-MPS-TTL	8
	Contact Signal Input	BLM-MPS-OPT	7
	Long-Distance Optical Transceiver	BLM-MPS-FCT	9
	CPU(IOC)	BLM-MPS-CPU	
	Power Supply	BLM-MPS-POWER	

Module ID check is carried out at the start-up time

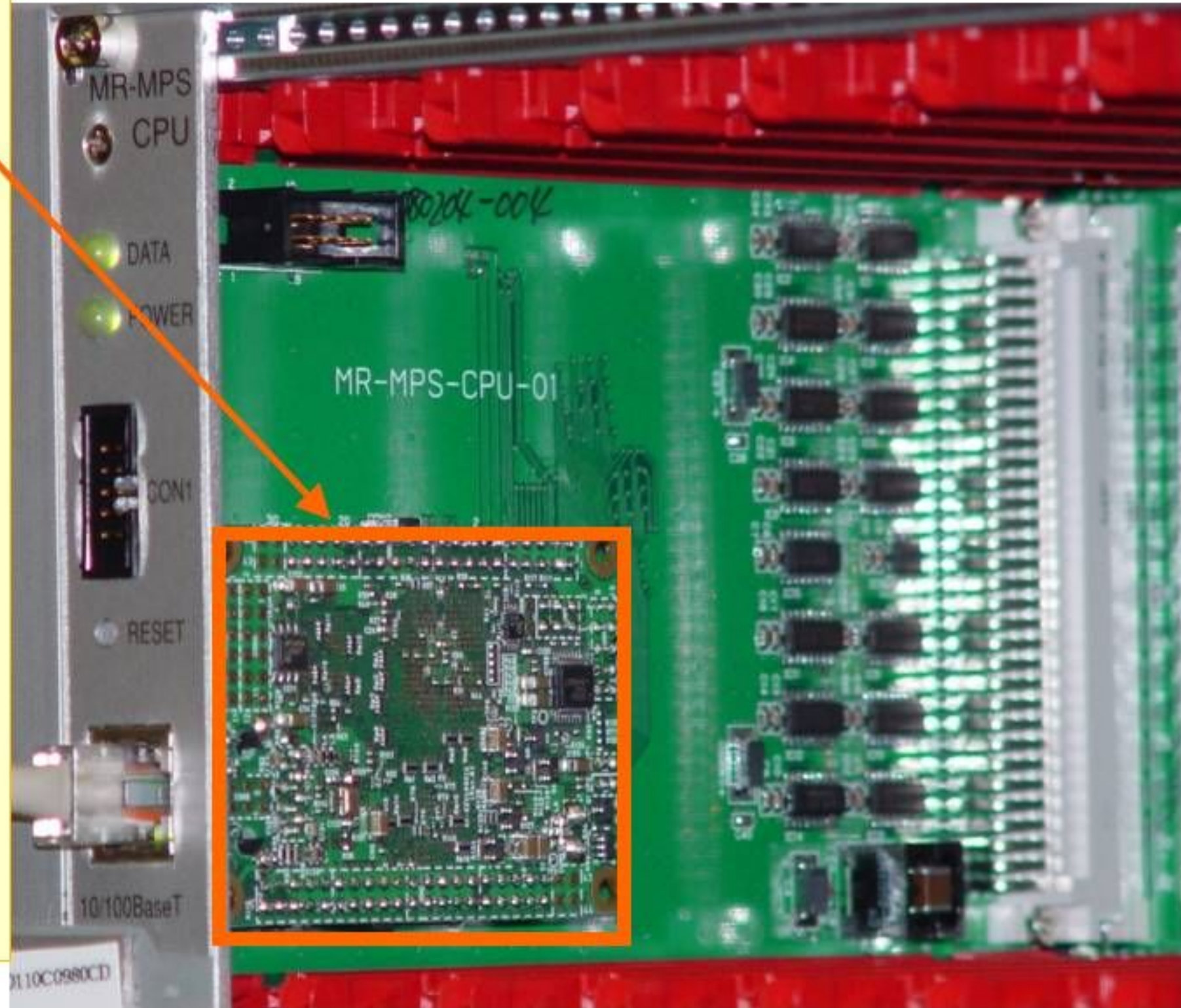
CPU module

SUZAKU

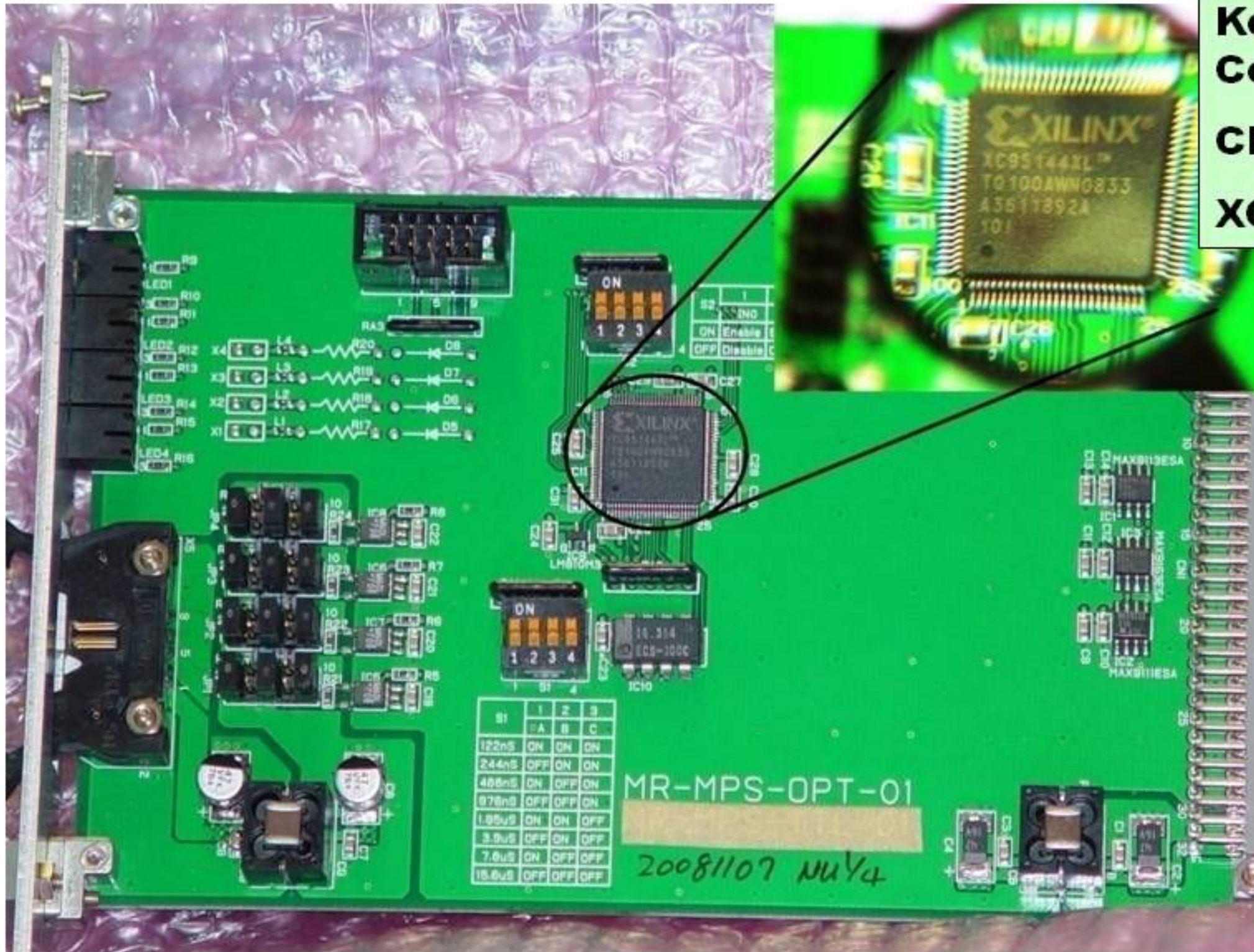
**Virtex-4 FX
XC4VFX12
(Xilinx FPGA)**

**CPU core:
PowerPC405
&
DRAM 64MB
Flash 8MB**

**# Commercial
products**

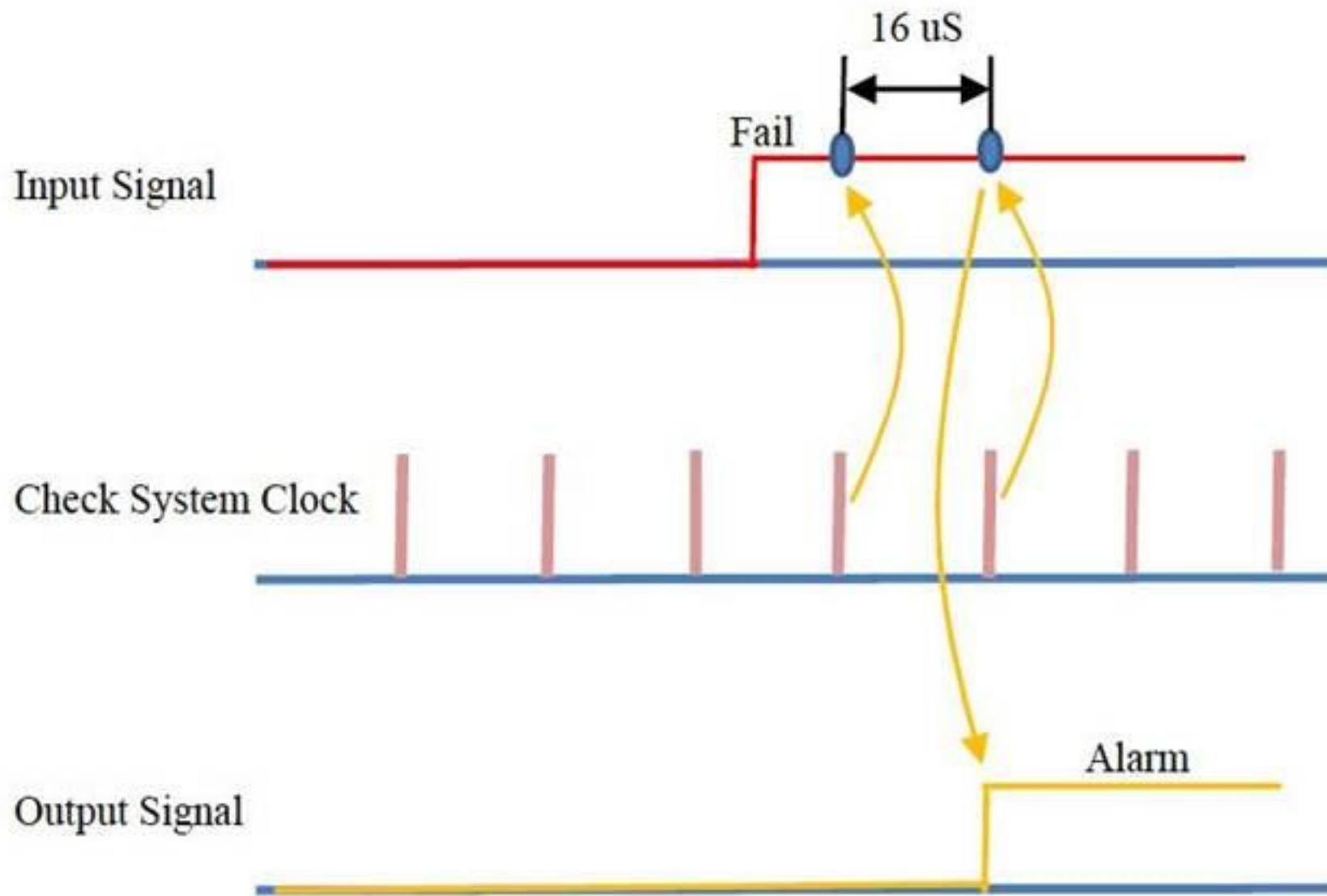


Contact Signal Input Module



**Key
Component
CPLD
XC95144XL**

Signal Confirmation (MR-MPS-OPT)

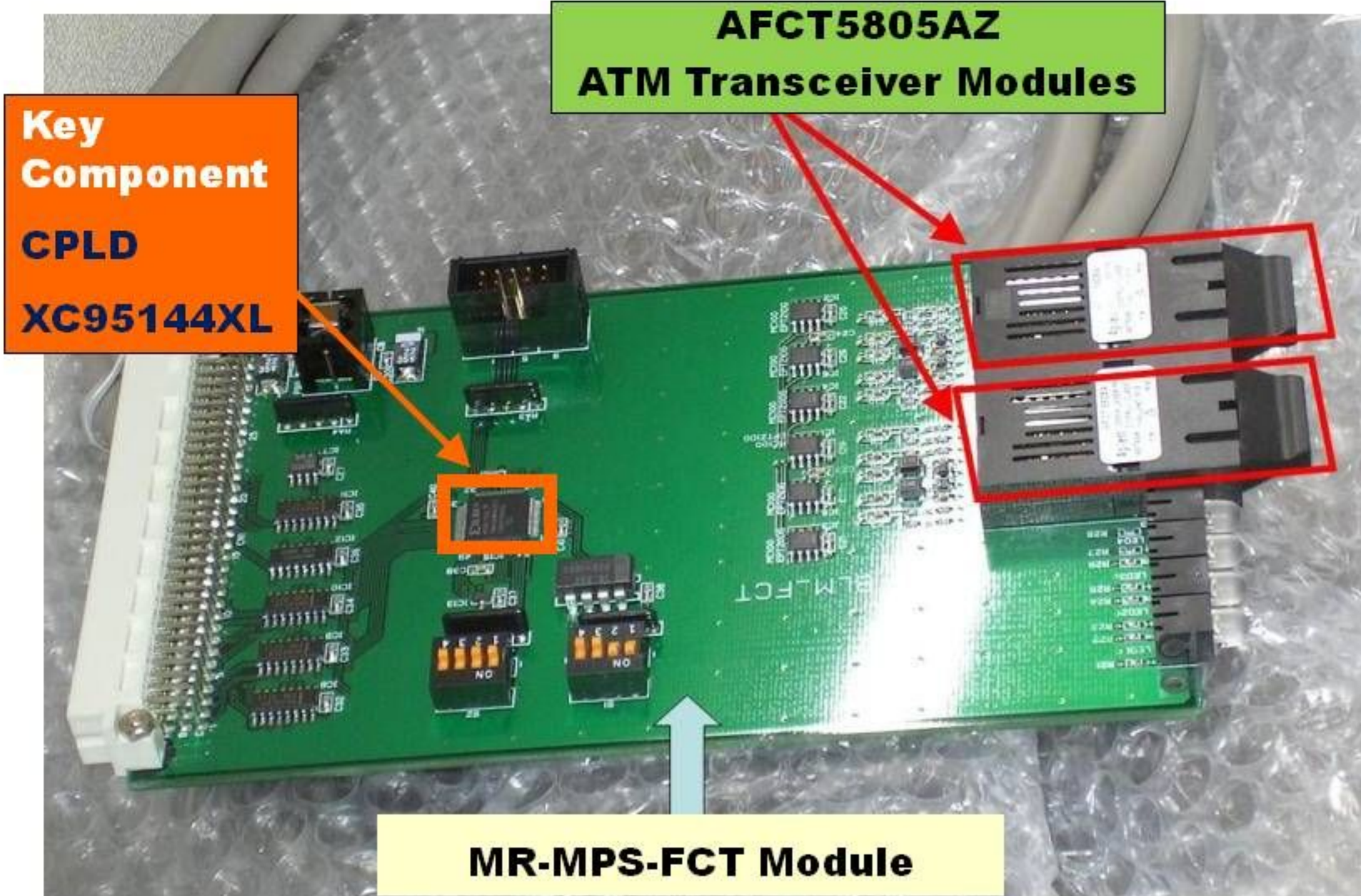


**Twice
check by
CPLD**

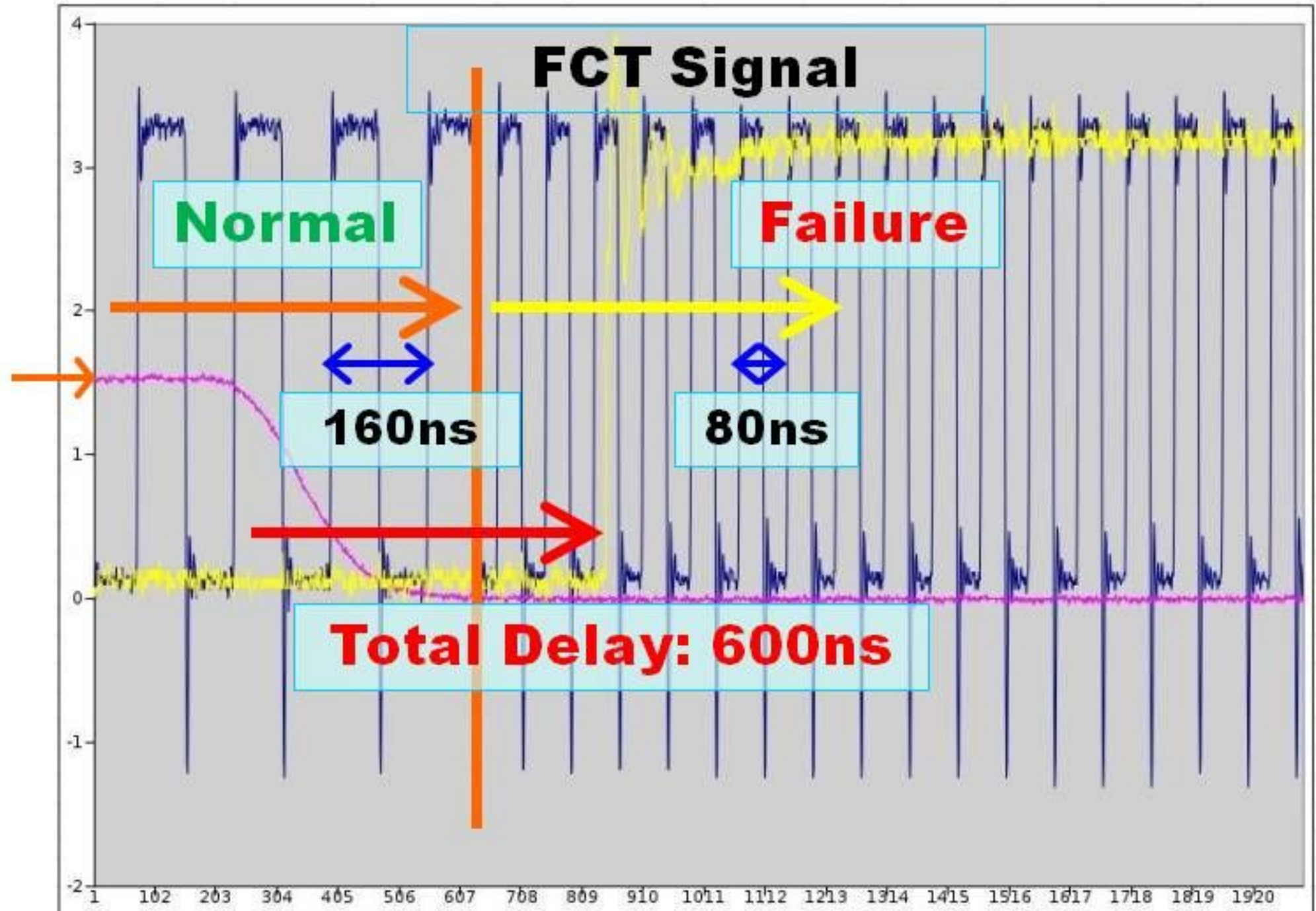
**=> High
reliability**

**Second sampling after the 16 micro
seconds**

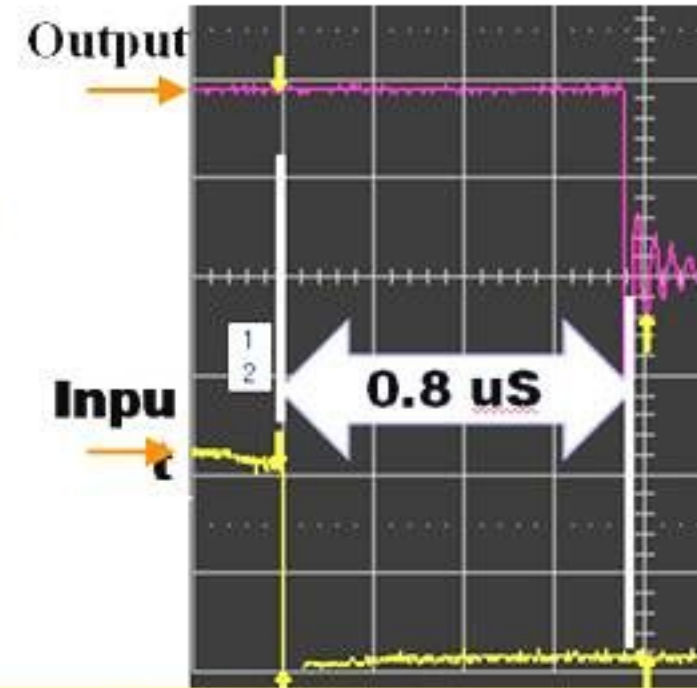
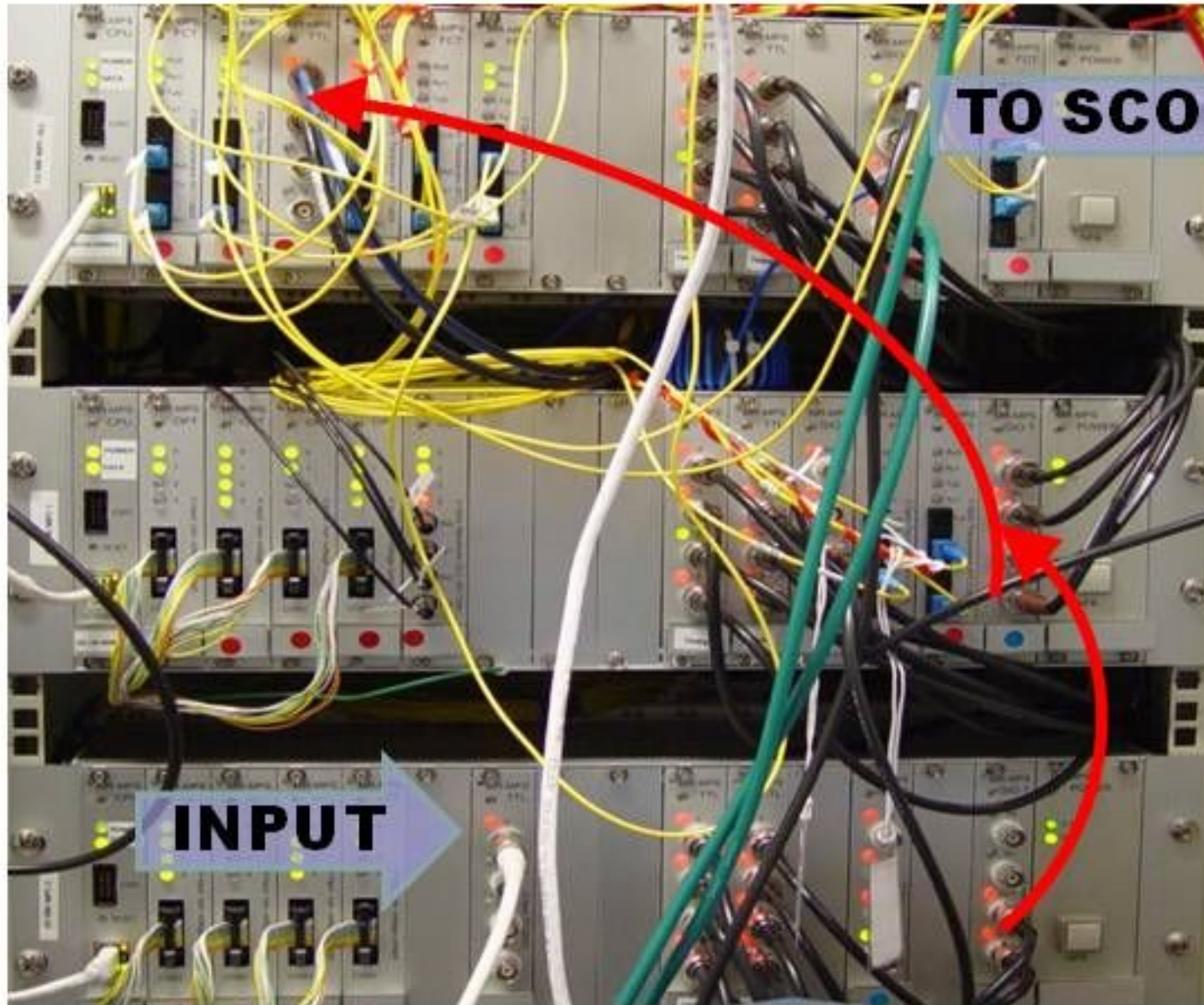
Link Module



Link Signal



Response Time



1) Subrack 3 stage

0.8 us

2) Inter-building

3-4 us

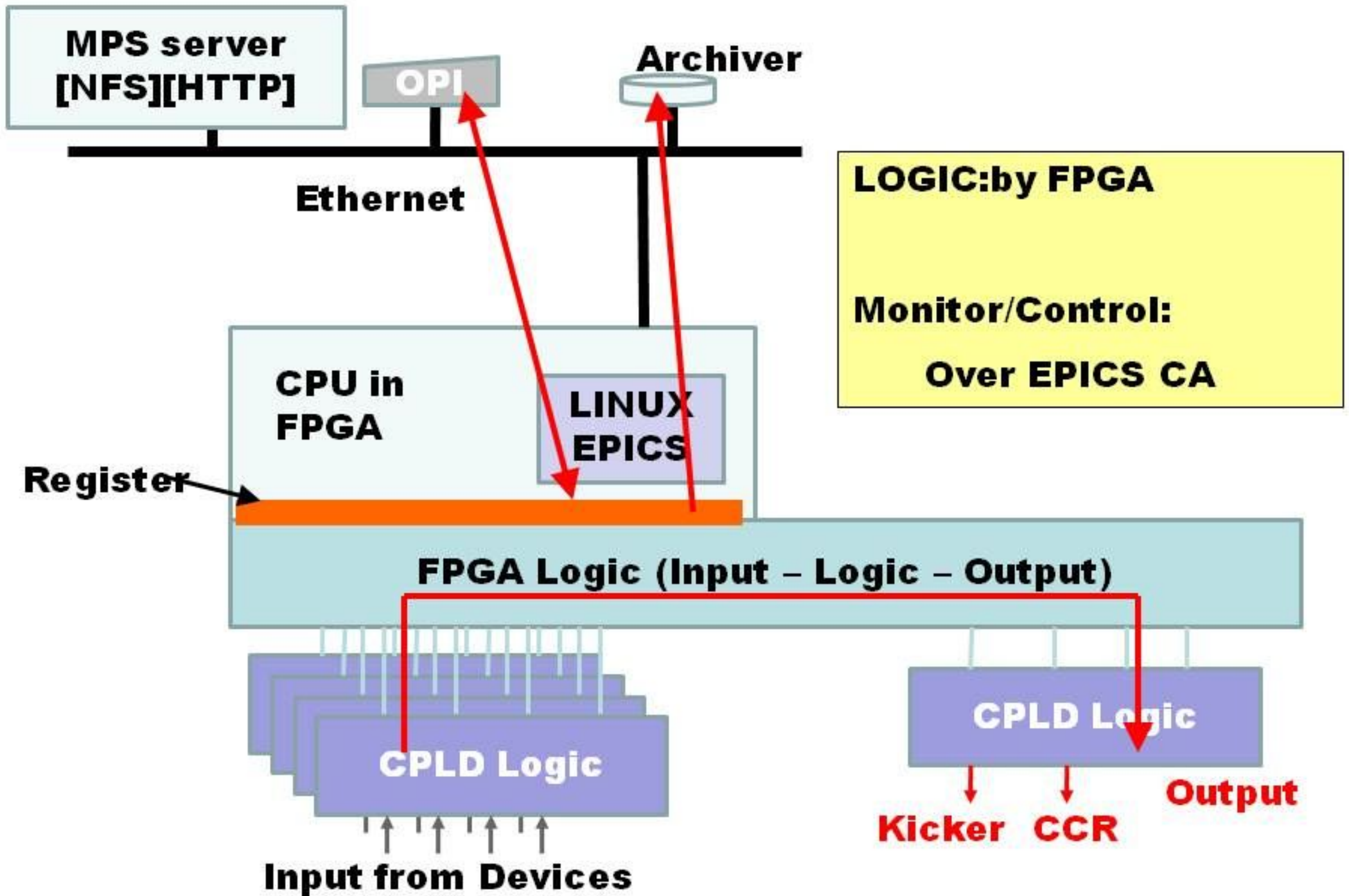
3) Link Module

0.6 us

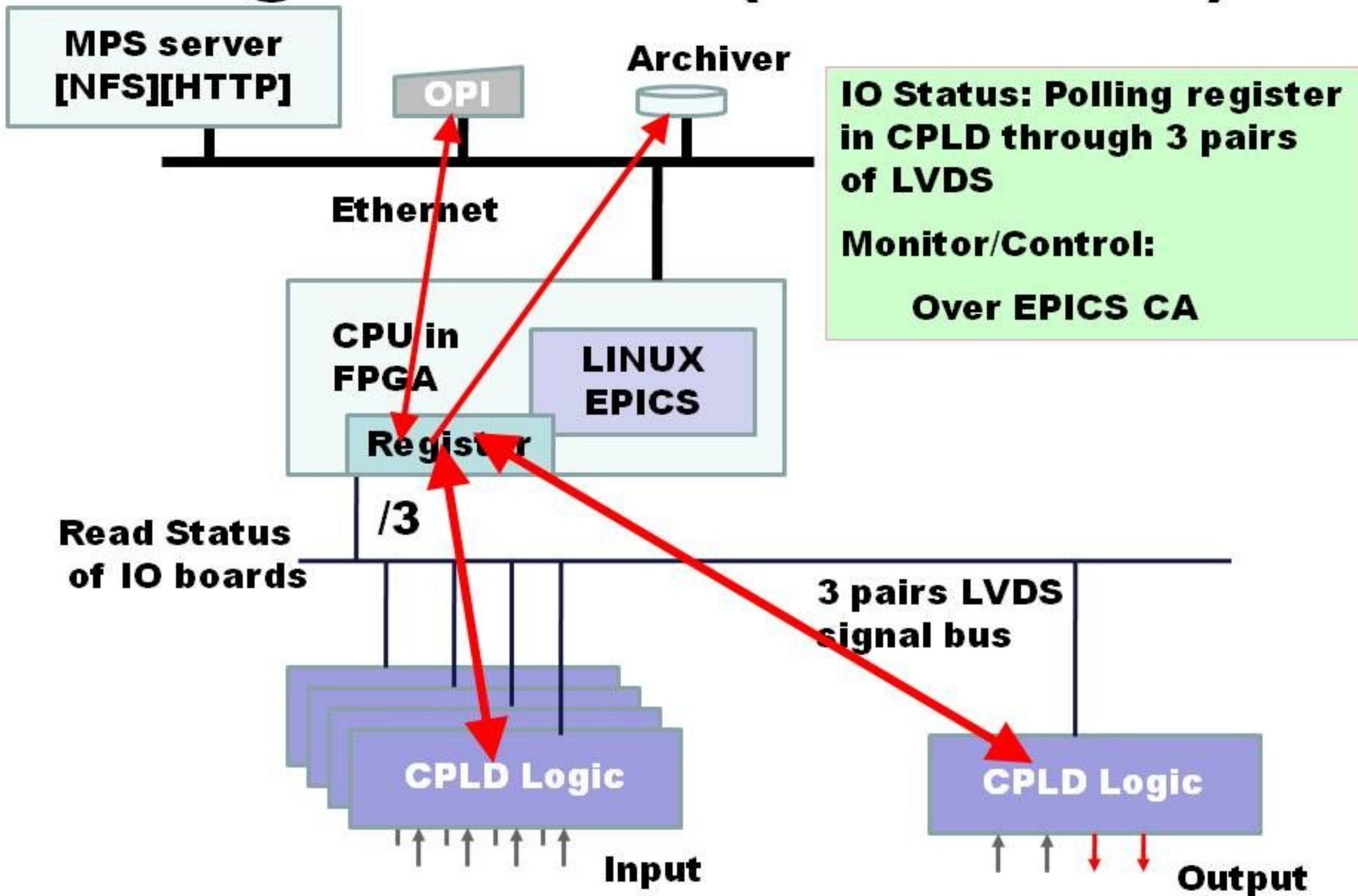
Total : about 6 us

Signal Handling for Quick Response and Maintainability

Signal Flow (Logic)



Signal Flow (IO Status)



Status Display for MR MPS

MR Summary

MR MPS Summary

Operation Stop

To CER
All MR

A B

Abort Request

Reset All

MR Devices BT Loss MR Loss Loss SP &

MR-MPS: Main Ring Devices

D1

- Loss 3-50 BT
- Loss MR
- Pulse Bend
- 350B-PS1
- 350B-PS2
- 350B-PS3
- 350BT-Vacuum
- Steering
- MR-Vacuum
- Inj-Sep1
- Inj-Sep2
- Inj-Kicker1
- Inj-Kicker2
- Inj-Kicker3
- Inj-Kicker4
- Inj-Bump1
- Inj-Bump2
- Inj-Bump3
- Dump-Sep
- Dump-Kicker1
- Dump-Kicker2
- Dump-Kicker3
- Dump-Kicker4

D2

- MainPS A-Stop-1
- MainPS A-Stop-2
- MainPS B-Stop-1
- MainPS B-Stop-2
- QFP
- QFT
- QDR
- SDB
- QDT
- QFS
- SFA
- SDA
- QDS
- QFR
- BMS
- BM4
- 3-50BT Fast CT

D3

- Loss MR
- Steering
- MR Vac
- MainPS A-Stop-1
- MainPS A-Stop-2
- MainPS B-Stop-1
- MainPS B-Stop-2
- FXAbt-Sep162
- FXAbt-Sep30
- FXAbt-Sep31
- FXAbt-Sep32
- FXAbt-Kicker1
- FXAbt-Kicker2
- FXAbt-Kicker3
- FXAbt-Kicker4
- FXAbt-Kicker5
- Abort-Q
- PPS
- BM1
- BM2
- QDX
- QFX
- RF-HV1
- RF-HV2
- RF-HV3
- RF-HV4

D2 Status Summary:

- Loss MR
- Steering
- MR Vac
- MainPS A-Stop-1
- MainPS A-Stop-2
- MainPS B-Stop-1
- MainPS B-Stop-2
- SX-Bump1
- SX-Bump2
- SX-Bump3
- SX-Bump4
- SX-ESS1
- SX-ESS2
- SX-Sep1
- SX-Sep2
- SX-Sep31-32
- SX-Sep33-34
- SX-EQ
- SX-RQ
- SX-Feedback

Reset All

30 66 102 138 174 210
 31 67 103 139 175 211
 32 68 104 140 176 212
 33 69 105 141 177 213
 34 70 106 142 178 214
 35 71 107 143 179 215
 36 72 108 144 180 216

Dispose

MR Devices

Operational Results

Month	Operating Hours	# of Shots	# of Equipments	# of Events	# of Malfunctioning
Jan	117	630	11	61	0
Feb	87	5194	4	6	0
March	0	0	0	0	0
April	81	2955	13	13	0
May	95	2764	5	13	1
June	122	3484	2	2	0
Total	502	15027	35	95	1

- **One event tells conflict of MPS display and condition of the equipment.**
- **95 events are detected in 500 hours of operation successfully.**

Summary

- **The MR MPS was developed using Virtex-4(FPGA) in the module structure.**
 - **Response time < 10 us** **OK**
 - **High reliability by CPLD** **OK**
 - **Flexibility by FPGA & EPICS** **OK**
- **This MPS system has been used for J-PARC MR**
 - **500 hours since Jan. 2009**
 - **95 MPS events was handled in the successful.**
 - **Only 1 report tells conflict of MPS display and condition of the equipment.**

Members about MPS

- **A. Akiyama: Design about System**
- **J. Odagiri : MPS part of Loss Monitor**
- **Y. Katoh : Test (Main Job : Linac/RCS)**
- **H. Nakagawa : Operation of MPS(MR)**

N. Yamamoto, N. Kamikubota, T. Kato

H. Yoshikawa, H. Sakaki

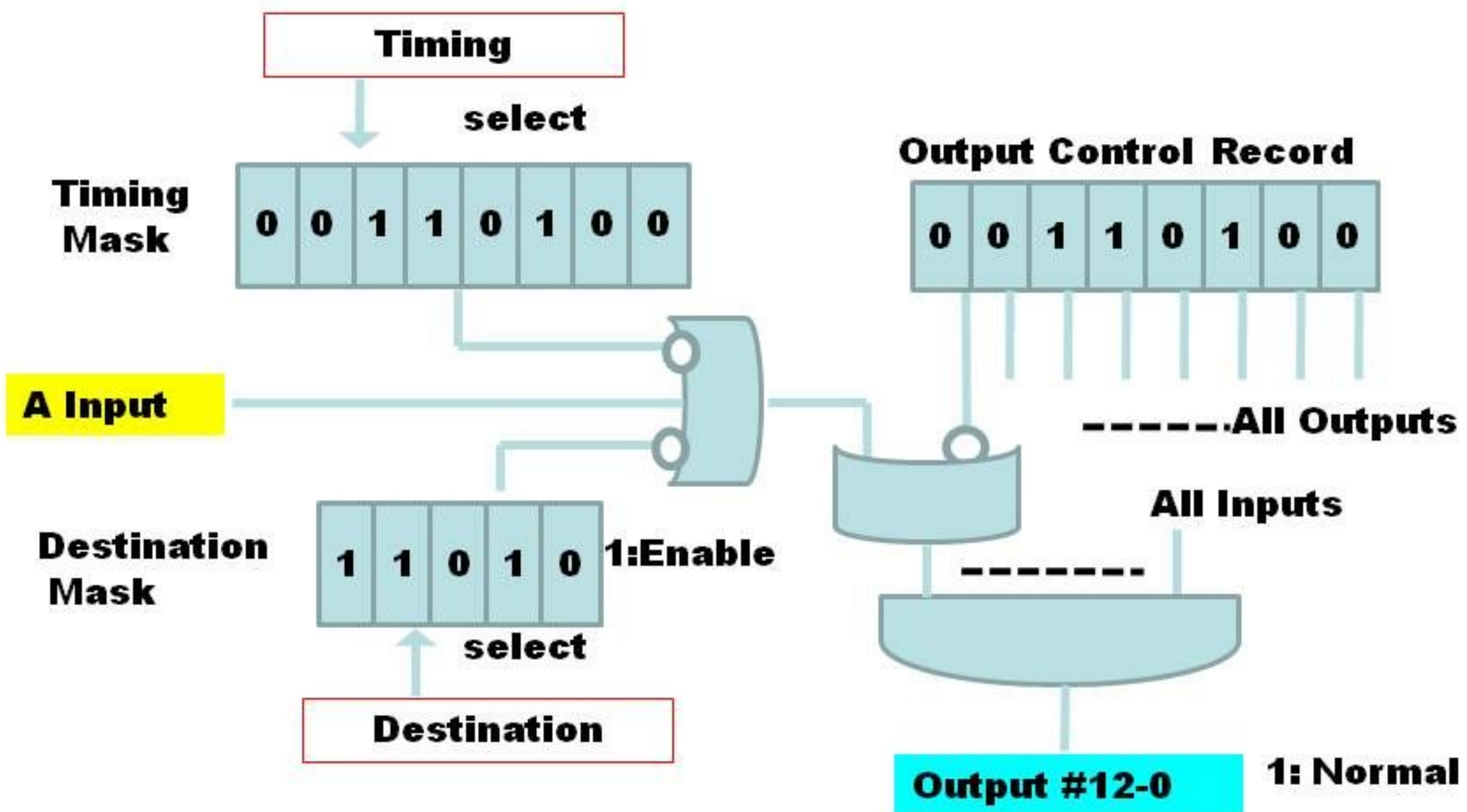
Beam Monitor Group

We can get enough power by this system for MPS.

2 kinds of Signal Masks

- **SW (in Modules)**
 - **Semi-rigidity (Field setting)**
 - **Everlasting**
- **Register (in FPGA)**
 - **Alterability from the central control room**
 - **Result is changed based on one destination**
 - **Temporary change returns to the default in the reboot**

Input & Output Mask (Register)



EPICS Environment etc.

- **FPGA Development: EDK (Windows XP) [VHDL]**
- **Soft Development: ATDE(VMware on WindowsXP)**
 - **LINUX: Ver. 2.6.18 (Deb. 4.1...)**
 - **GCC: Ver. 4.1.2**
 - **EPICS: 3.14.9**
 - **Homemade Register Control Driver**
- **Files on Server: NFS mount**
 - **Base, DB, etc.**
 - **Copy to RAM disk, if need**
- **OPI: MEDM**
- **Archive: camonitor etc**

Operation Statistics

Month	Operaton (h)	Shot	Devices	MPS Counts	Confirmation need
Jan.	117	630	11	61	0
Feb.	87	5194	4	6	0
Apr.	81	2955	13	13	0
May	95	2764	5	13	1
Jun.	122	3484	2	2	0
Total	502	15027	35	95	1

The report of misoperations and equipment tests etc. is not counted.