ORION Gateway Design for Feedback Controls Connectivity

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ORION Introduction

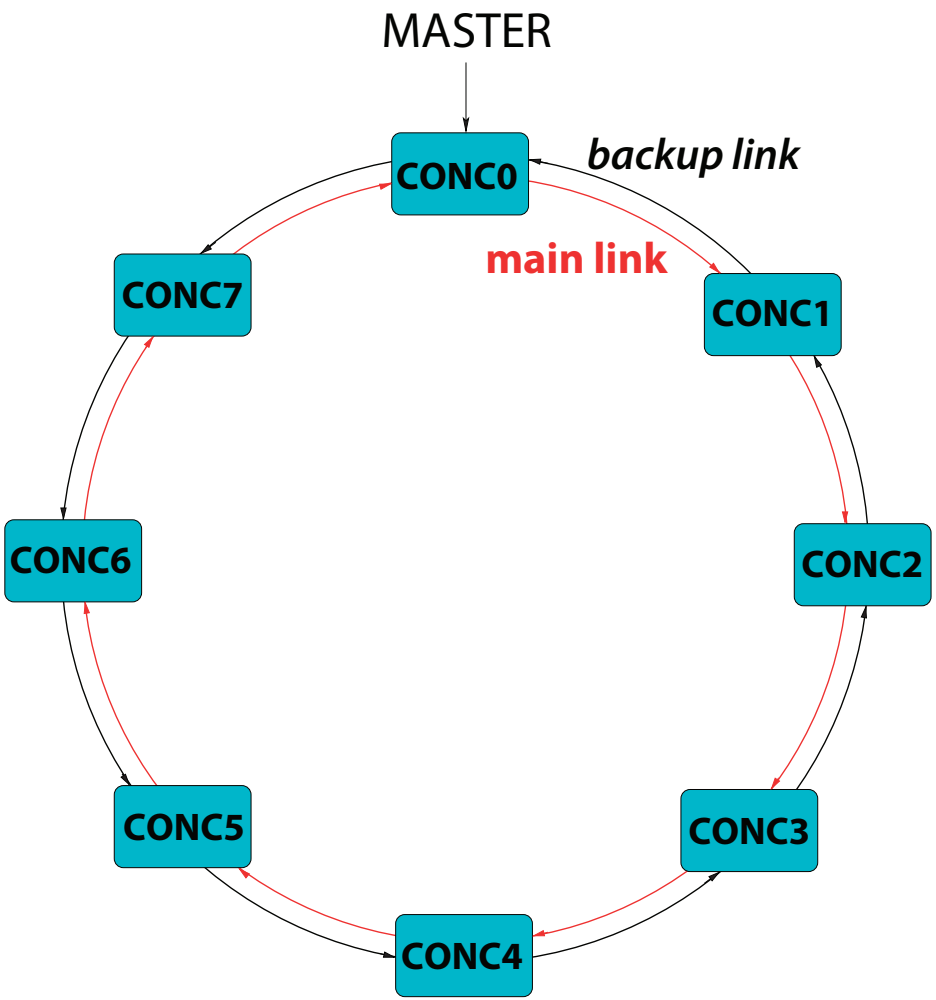
ORION = Optical Redundant Input/Output Network

- One FPGA per sector, linked with fiber optics
- All FPGAs operate on a common clock frequency
- Periodically ($\sim$10 kHz) communicates BPM data (or other hard-real-time accelerator info) from every node to every other node
- Assume computation (e.g., feedback equation

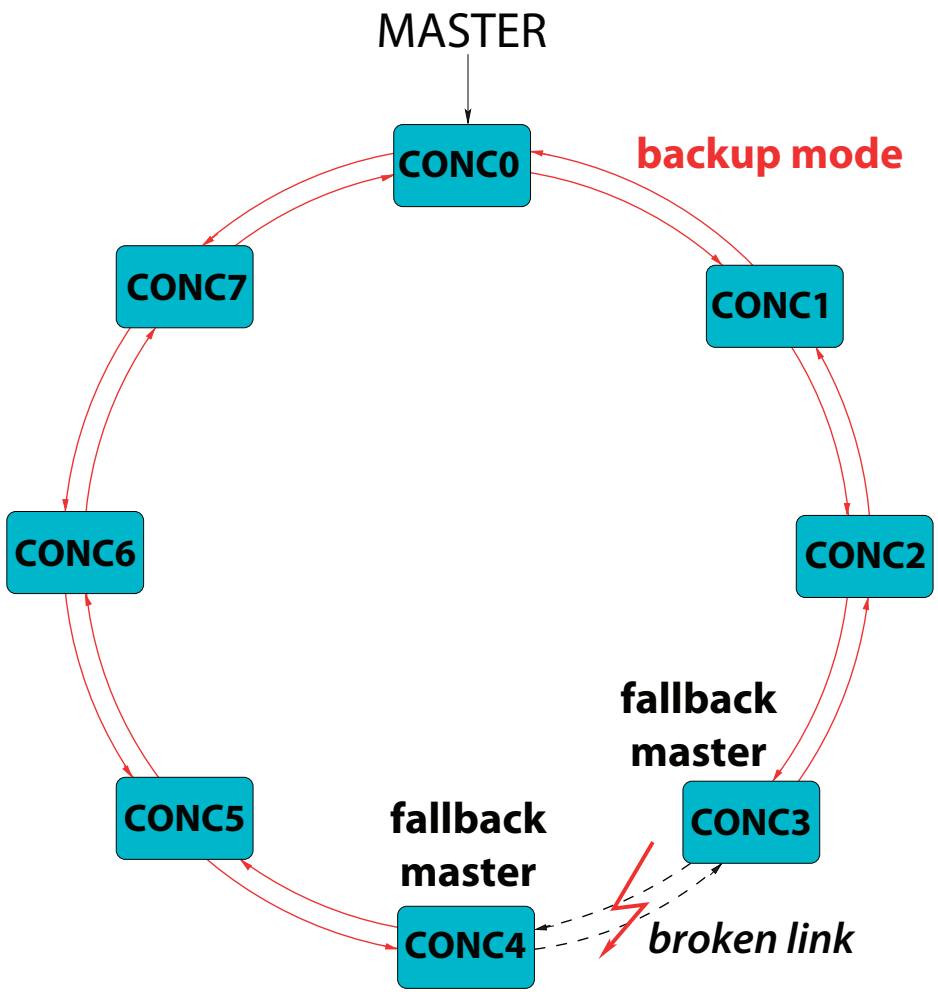
$$B = \int \mathbf{A} \cdot (x - x_{SET})$$

) will also be part of FPGA
- Fault-tolerant ring

ORION ring network: Normal operation mode

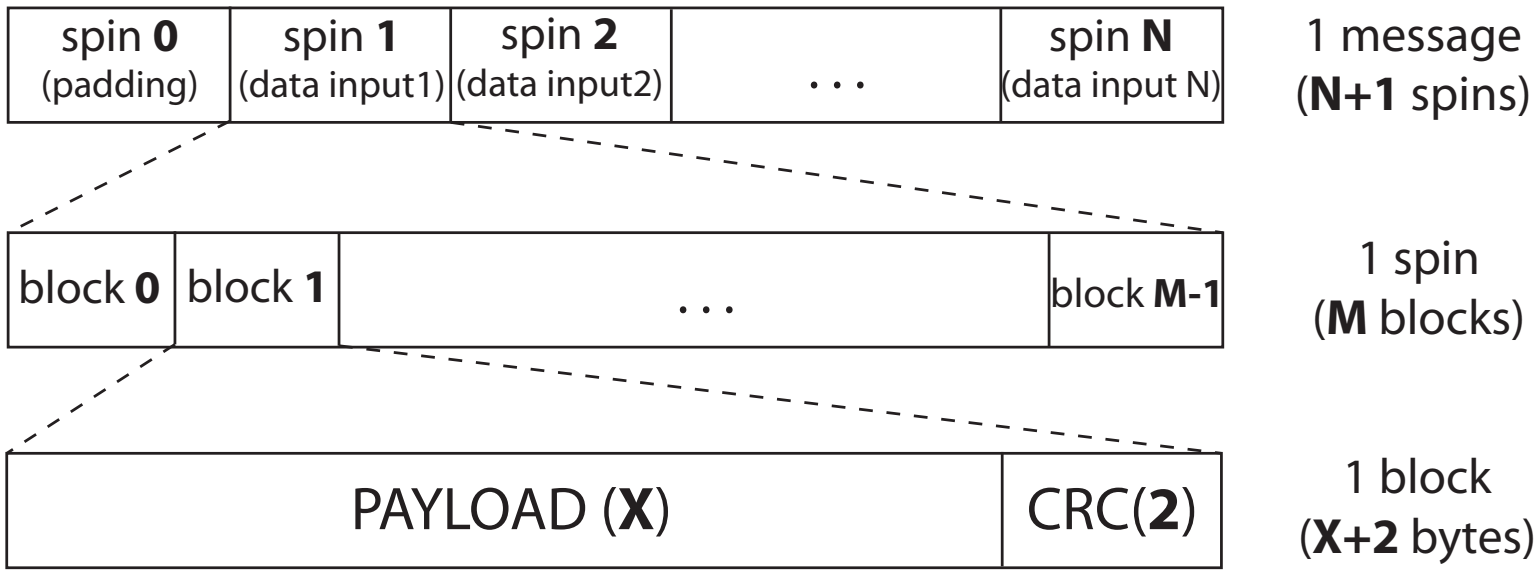


ORION ring network: Fault recovery mode



Structure

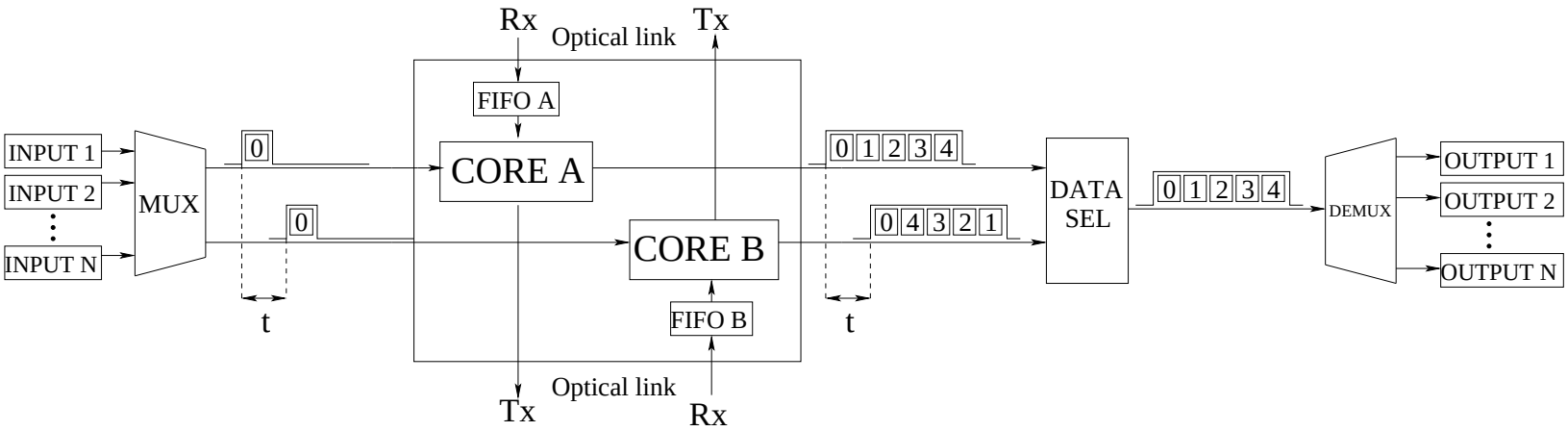
- Message structure and terminology



- Repeated every 100μs or so
- One block comes from one node
- M = number of nodes

I/O interfaces

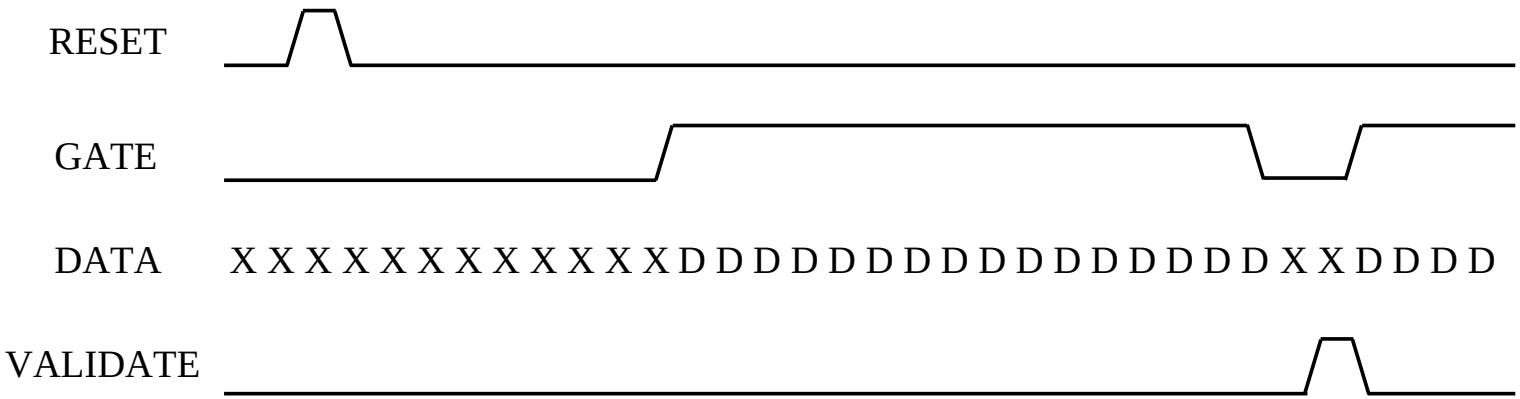
- Functionality of one node (out of ∼30)



- FIFO tuned so one propagation time through node is exactly the length of one block.

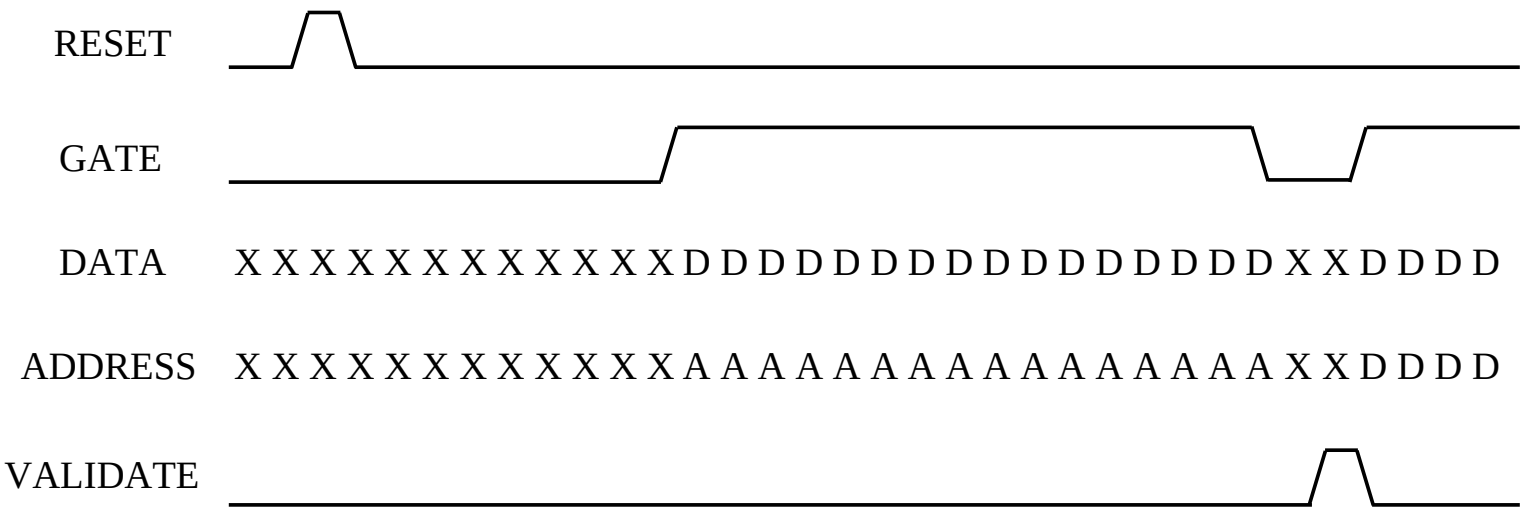
Input timing diagram

- All nodes and all spins provide reset at the same time (plus or minus one clock cycle)
- Data introduced into the network while provided gate is set
- Data input bus doubled for *a* and *b* links
- X represent don't care and D series of octets in payload



Output timing diagram

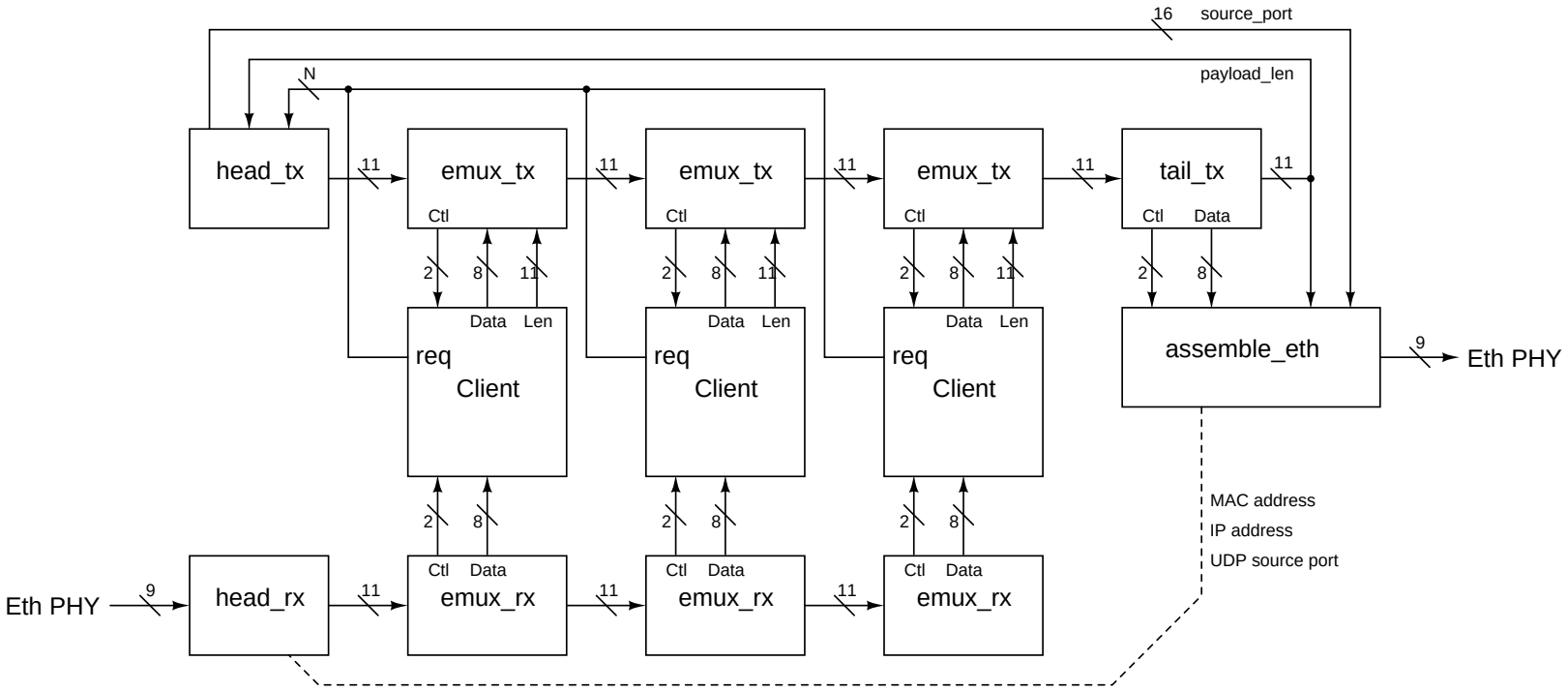
- Same interface as the input except for an address and validate
- Validate derived from CRC checks
- Address word gives spin number and origin node number for the payload



Ethernet access

Pseudo-Scalable Pseudo-Ethernet Pseudo-Switch

(Short-tick FPGA targeted, 2-16 clients, UDP payload, one to many and many to one switch)



Status 2009-09-27: validated in hardware using simple test clients

Full-rate GigE in about 1k FPGA logic cells

No ARP yet

Results

Architectural features

- Deterministic and synchronous (jitter-free)
- Low latency (no computers in real-time path)
- Fault tolerant
- Flexible
- Scalable

Prototype running on a laboratory scale

- Demonstrated fallback operation when a fiber optic cable is unplugged
- Demonstrated recovery to normal state when fiber is restored
- No human or computer intervention needed

Conclusions

- A common clock and commodity telecom parts make high speed, deterministic communications with an FPGA easy
- Fault tolerance takes serious effort

Acknowledgements

- Motivation and support from Bob Dalesio (BNL)

Thank you!

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