THE CONTROL SYSTEM FOR INDUCTION ACCELERATION IN THE KEK DIGITAL ACCELERATOR

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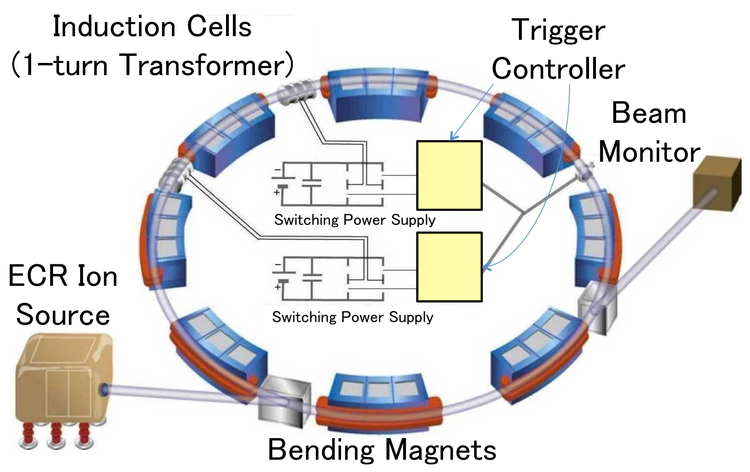
Introduction

A digital accelerator (DA) is a low energy version of the induction synchrotron which has been demonstrated using the KEK 12 GeV-PS in 2006. The DA is injector-free and its acceleration and bunch confinement are independently carried out by induction cells, which are 1-to-1 transformers driven by individual switching power supplies employing high power and fast semiconductor switching devices (MOS-FET). These devices allows us to realize a so-called all-ion accelerator. A full digital control system of the KEK-DA is under development. It consists of an FPGA and a communication interface to produce current signals for induction cells to accelerate beam ions according to the trigger signal from a bunch monitor.



The outline of KEK-DA

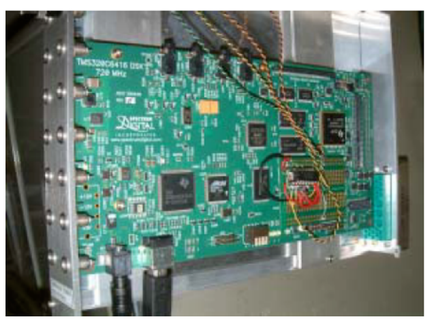

KEK-DA

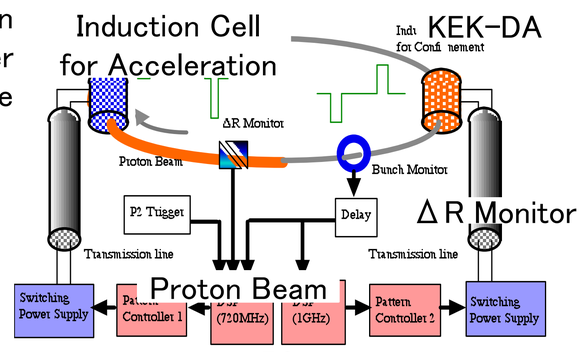
Present control system

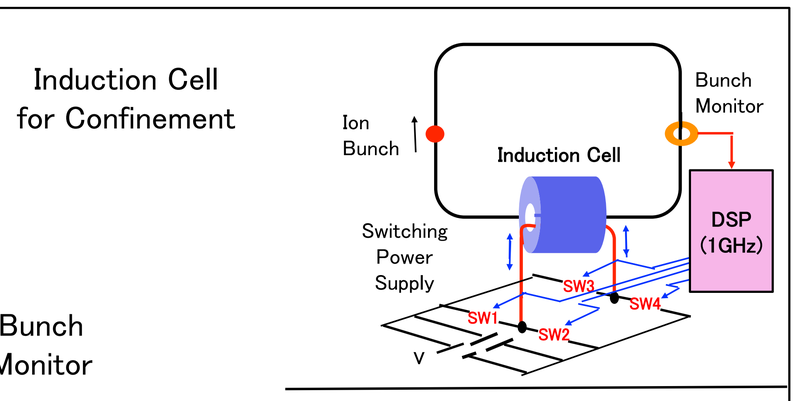
- The induction acceleration system consists of the 9.4GHz electron cyclotron resonance (ECR) ion source, induction cells, switching power supplies, DC power supplies and the DA control system to drive the switching power supplies.
- The switching power supplies are controlled by eight DSP modules.

DSP module

- The specifications of the DSP modules are as follows;
  DSK6416T(Texas Instr.)
  32-bit timers
  clock frequency 128MHz
  C-language.
- Each DSP board produces current signals for each induction cell to accelerate beam ions according to the common trigger signal from the bunch monitor.



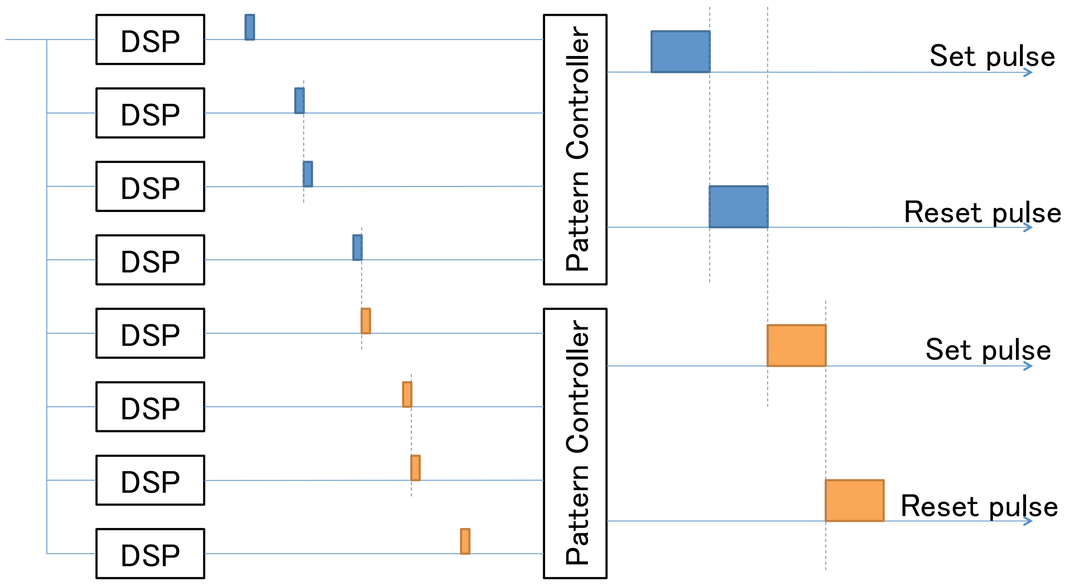




DA Control System

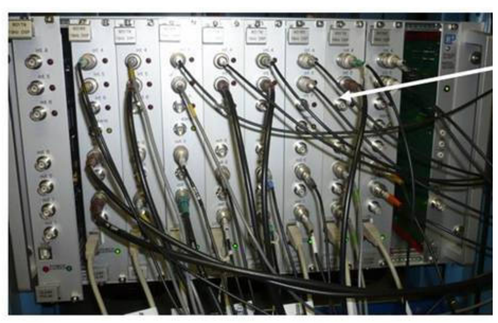
Advanced control system

Present system

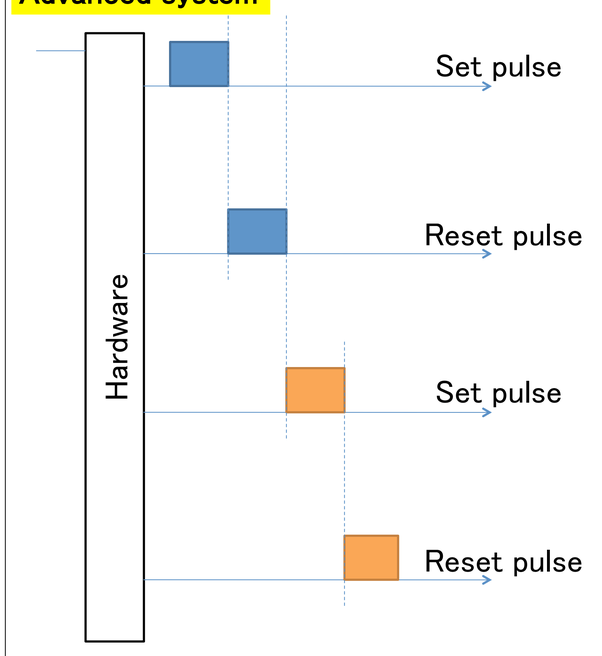


The block diagram of the present control system

- The present control system is easy to change the software program to modify the control method.
- The eight DSP modules and PCs are large enough to a 19 inch rack.
- In the present system the eight DSPs are executing same program individually loaded by a computer
- The DSP modules can not communicate each other.
- To realize variable acceleration pulse lengths, start/stop timing of acceleration voltage must be intelligently controlled turn by turn.
- The first pair of induction voltage (blue signals) is for the first cell and the second pair (orange signals) is for the second cell.

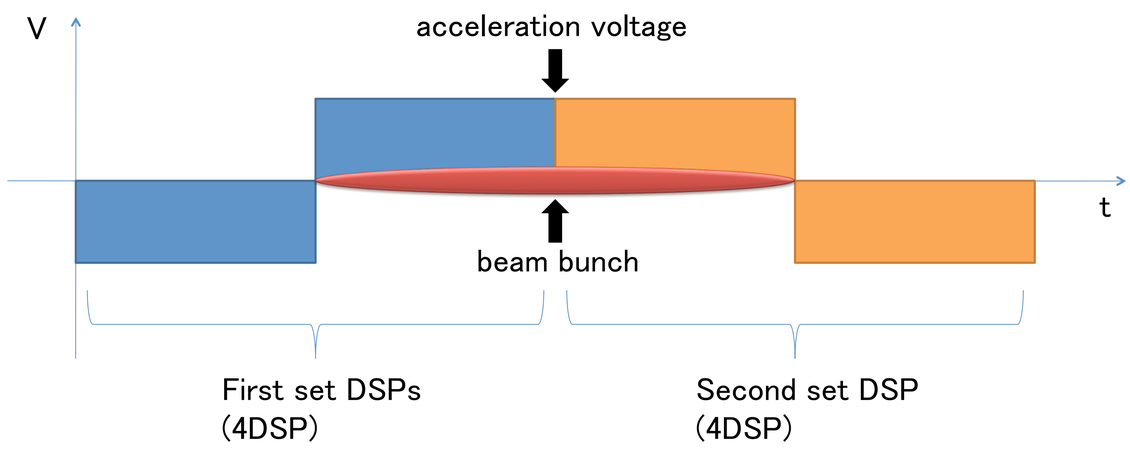

8 DSP modules

Advanced system



The block diagram of full digital control system

- The FPGA produces four digital signals for induction cells.
- The system becomes very compact
- Its processing time will be improved by parallel processing and arithmetical computation technique using lookup table memories.
- The single FPGA simplifies the hardware circuit and it is very effective to scale down the control system and easy to change the operating parameters.



The relation between voltage of the IC and timing pulses from the DSPs

The merits and demerits of the present system and the advanced system

	Merits	Demerits
Present system	・Easy to change program	・Over spec
Advanced system	・Speed up ・Compact ・Saving resources	・Need hardware skill

Future Plan

- To select an evaluation board implemented by an appropriate Xilinx FPGA device and install Verilog HDL program developed by ISE foundation.
- To make simulation test using a pulse generator.
- To compare the performance with the present system.