Commissioning of the FPGA based Transverse Feedback System at the APS*

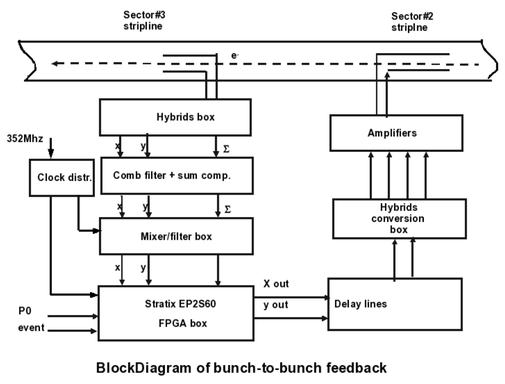
Abstract:

The Advanced Photon Source installed a Transverse Feedback System to correct the instability in the electron beam during single bunch mode. This instability manifests itself when a large amount of current is present in the beam. The only method formerly available to correct the instability was through chromaticity correction. The transverse feedback system deals with the instability without requiring changes to the ring chromaticity. Initial testing revealed issues with the input and output electronics. This paper will discuss these issues, their resolution and many other enhancements to the FPGA-based system.

1. Storage Ring @ 352MHz, (2.84ns)
2. Bunches/buckets = 1296
3. ADC sampling rate 117.33 MHz (8.52ns)
   a. Samples a ⅓ of the buckets.
   b. 432 buckets can be enabled.
4. Storage Ring turn rate = 271.6kHz (3.68μs)
5. Inputs use 14-bit A/D
6. Output uses 14-bit D/A

The X-plane output at the main box may be used for diagnostics, or be used to drive the tune measurement system.

System Block Diagram



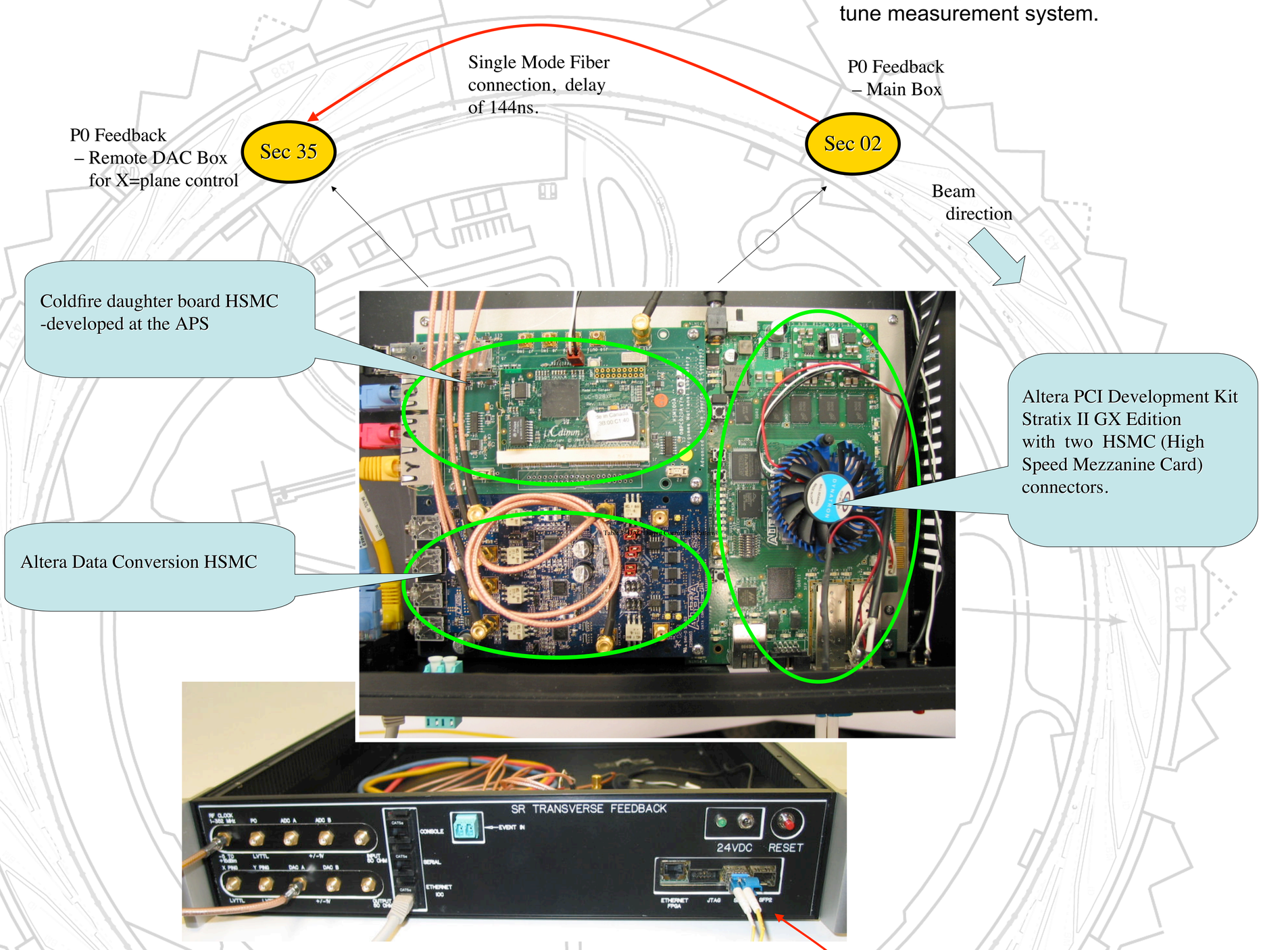
BlockDiagram of bunch-to-bunch feedback

The front-end input circuit was upgraded from the monopulse receiver to a 3-tap comb filter.

Bucket Output control

000	Zero volts out
001	Normal processed data out
010	Negate processed data out
011	Programmable negative output value
100	Programmable positive output value
101	Toggle (negate) data from previous bucket
110	Stretch (repeat) data from previous bucket
111	Zero volts out

Each of the 432 buckets can be controlled individually for purposes such as timing alignment, AC coupling effect compensation of DAC output, and bandwidth matching for the amplifiers

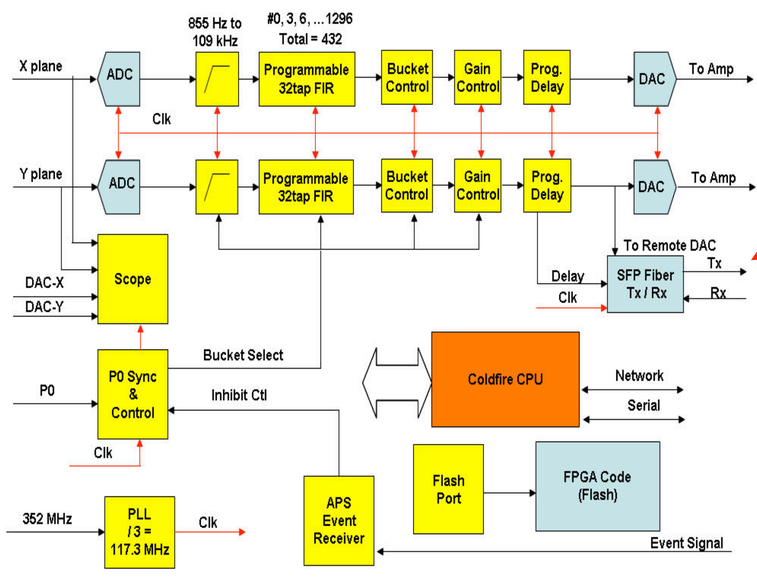


Remote Fiber Optic link

The remote DAC is connected via a 2.34 Gb/s fiber optic. The transmitter at the main box is in 16-bit mode while the receiver at the remote DAC box is in 8-bit mode. The 8-bit mode is used to solve two issues, 1) byte swapping that may occur at power-up or if fiber was disconnected and 2) the need to half step the delay value being sent to the remote DAC.

-- Transmitter using 117.333 MHz reference clock.
-- Receiver using 234.666 MHz reference clock.

FPGA Main Block Diagram



The heart of the FPGA is the 32-tap FIR filter. Both the X-plane and Y-plane have 432 individual 32-tap FIR filters with each element being 18-bits wide. Each plane uses a common coefficient register for all 432 filters. The computation speed for all 864 filters is greater than 7.5×10^9 multiply-accumulate operations per second.

P0 Feedback and Remote DAC Hardware

1)Altera PCI Express Development Kit Stratix II GX Edition
   a)Two SFP (small form-factor pluggable) cages, one used fiber optic transceiver.
   b)Two HSMC (high speed mezzanine card) connectors
2)Altera Data Conversion HSMC
   a)Two Analog to Digital converters, 14-bits @150 Ms/s
   b)Two Digital to Analog converters, 14-bits @ 250 Ms/s
3) Coldfire CPU daughter board with HSMC connectors.
   a) Fiber optic transceiver used for the event timing system.
   b) Console, serial and ethernet ports, RJ45
   c) Connector for an RF clock, which directed to the FPGA.
   d) User defined SMB connector, 2 inputs and 2 outputs.
4) Transceiver by Finisar, model FTLF1324P2BTL
   a) A 4Gb RoHS Compliant Long-Wavelength SFP Transceiver

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