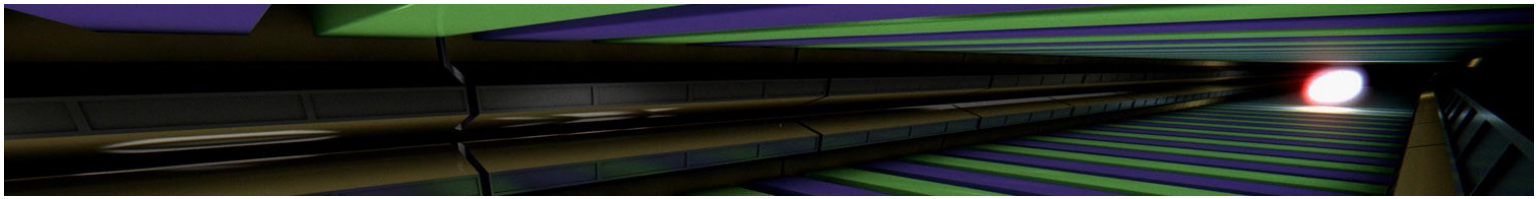


ICALEPCS 2009

New Hardware and Software Developments for the XFEL

Kay Rehlich
on behalf of the XFEL controls group

Hardware & Software Evolution

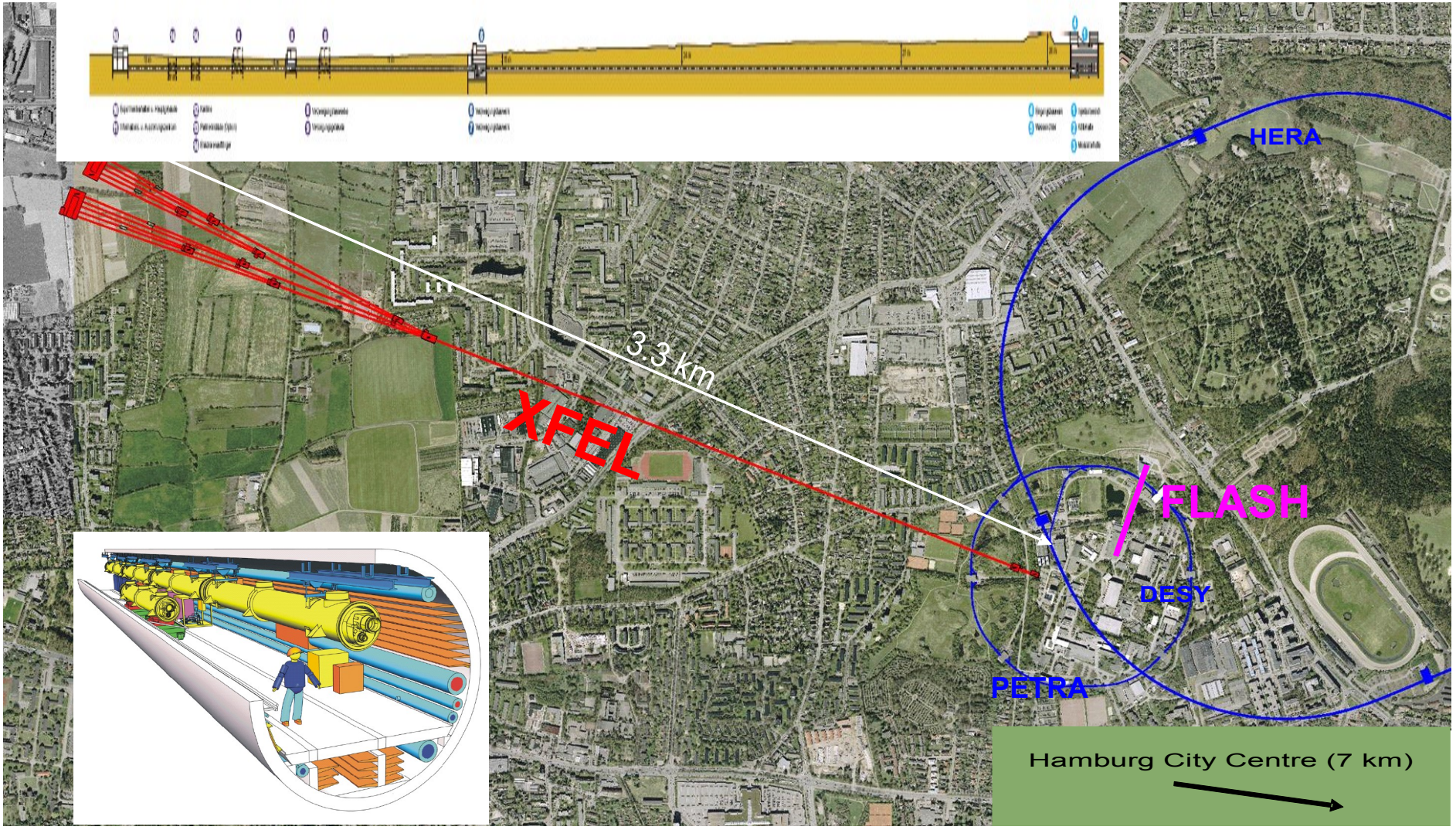
Since 2005
FEL User Facility
6 .. 32 nm

1993 — 2014

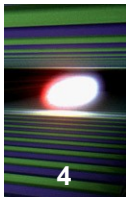
TTF → FLASH → XFEL

VME	Hardware →	xTCA
C++	GUI Programming →	JAVA

The XFEL Project



Evolution: VME → µTCA / ATCA



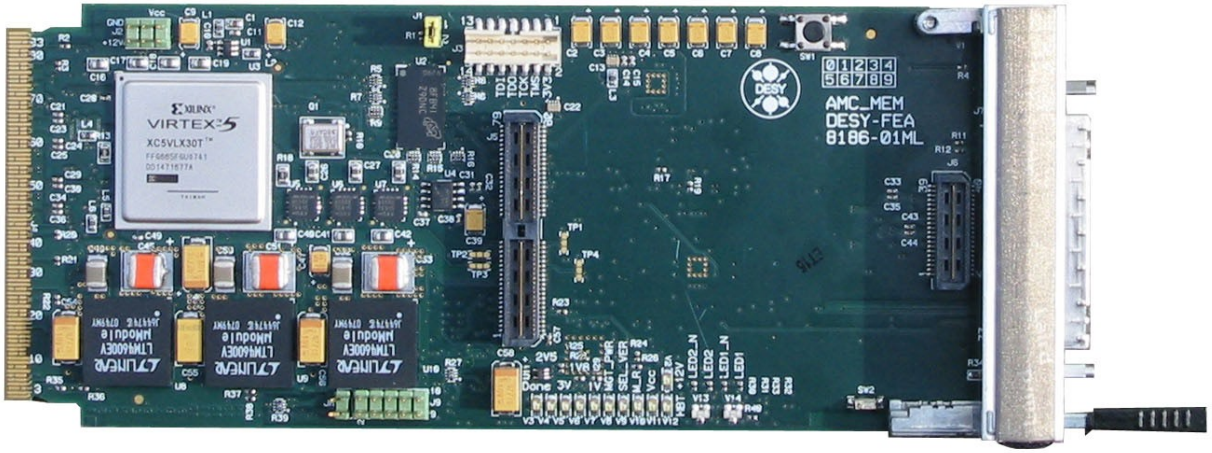
- **VME** is 27 years old:
  - Number of new developments is decreasing, sales are still constant
  - Bus technology has speed limitations
  - Wide busses create a lot of noise in analog channels
  - But, a lot of I/O modules are available
  - No standard management on crate level
  - No management on module level
  - So far no extension bus survived
  - One damaged bus line stops a whole crate
  - Address and interrupt misconfigurations are hard to find
  - ....

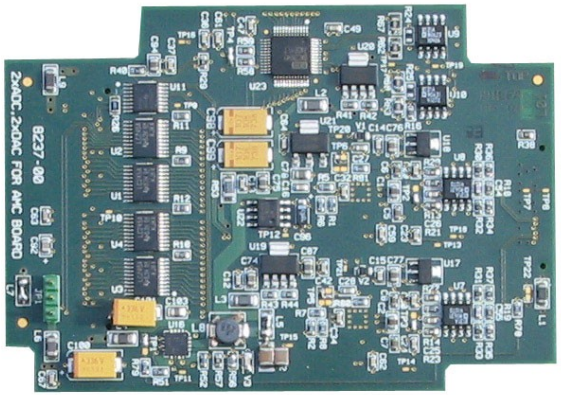
Evolution: VME → µTCA / ATCA

- Scaleable modern architecture
  - From 5 slot µTCA … full mesh ATCA
- Gbit serial communication links
  - High speed and no single point of failure
  - Standard PCIe, Ethernet (, SRIO) communication
- Redundant system option
  - 99.999% availability is possible
- Well defined management
  - A must for large systems and for high availability
- Hot-swap
  - Safe against hardware damage and software crashes

$$A = \frac{E[\text{Uptime}]}{E[\text{Uptime}] + E[\text{Downtime}]}$$

AMC Design (DESY)

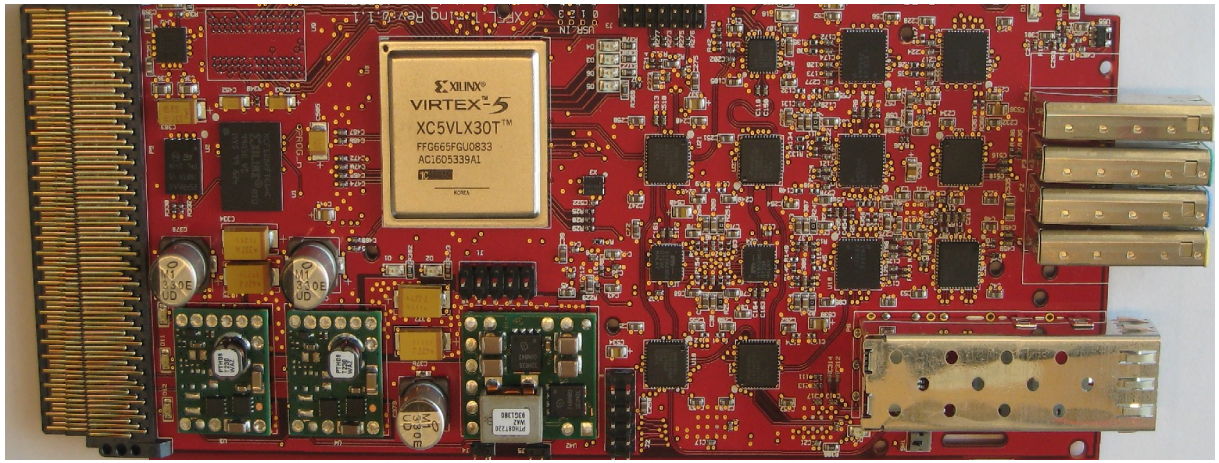




2 ch ADC, 2 ch DAC, 125MSPS

- Development of an 'universal' AMC module
  - Hardware design with Virtex5 and 256MB DDR2 SRAM (1GB/s)
  - FPGA code development with PCIe interface and DMA
    - ➔ 370 MB/s into user space (128byte payload size)
  - DOOCS server and OS driver incl. hot-swap
  - IPMI code for 'Module Management Controller' (Atmega-128)
  - Piggyback with 2 ADC and 2 DAC channels, 100MHz
- Tested @ FLASH: BPM and Toroid readout with 81 MHz

Timing AMC



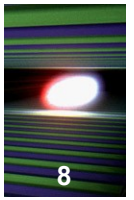
Clock and trigger OUT

Clock and data Fiber optic IN

- Development of a ps stable timing system
  - Clock, trigger, interlock and event distribution
  - Fiber optic links (3.5 km), 1.3 GHz telegrams
  - Goal: < 5 ps jitter, 1.54 ns trigger resolution
  - Drift compensation on ps level

UNIVERSITET STOCKHOLMS
FYSIKUM

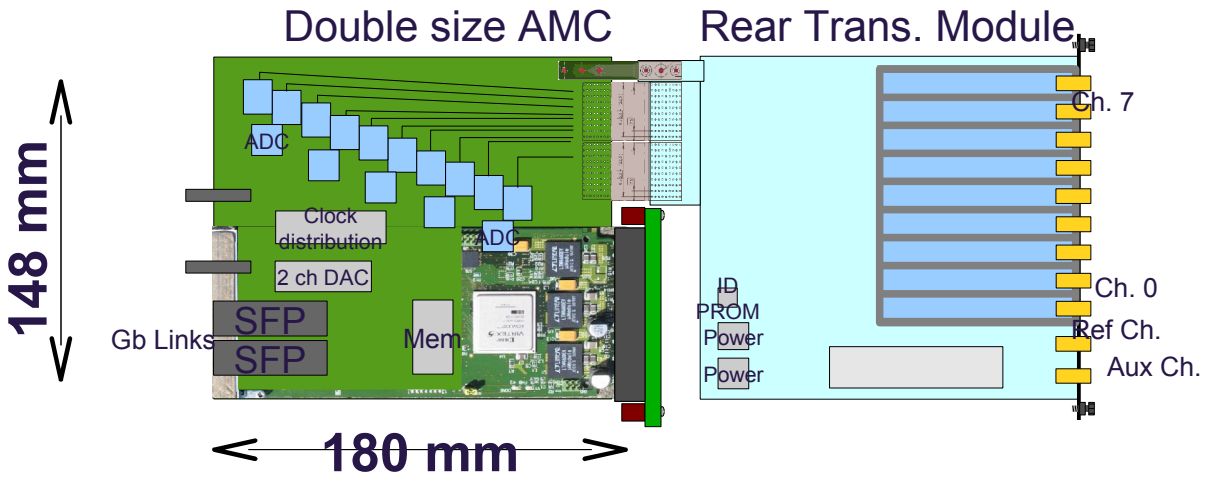
Results of the µTCA Evaluation



- We did it the hard way:
  - Crates, CPUs, IO and MCH from different vendors
- Management of crates is well defined
  - Dynamic module and crate info gives all relevant info
- Fast data transfers (>400MB/s on 4 lanes PCIe)
- Hot-swap (tested with Solaris and Linux)
  - hardware is controlled by the MCH
  - software reconfiguration of OS PCIe drivers
- Good decoupling of modules on the backplane
- Good analog performance
- µTCA standard requires a few additions
  - The specs are made for telco, customized solutions, we want COTS → xTCA for Physics @ PICMG

→ xTCA platform is a good basis for large installations

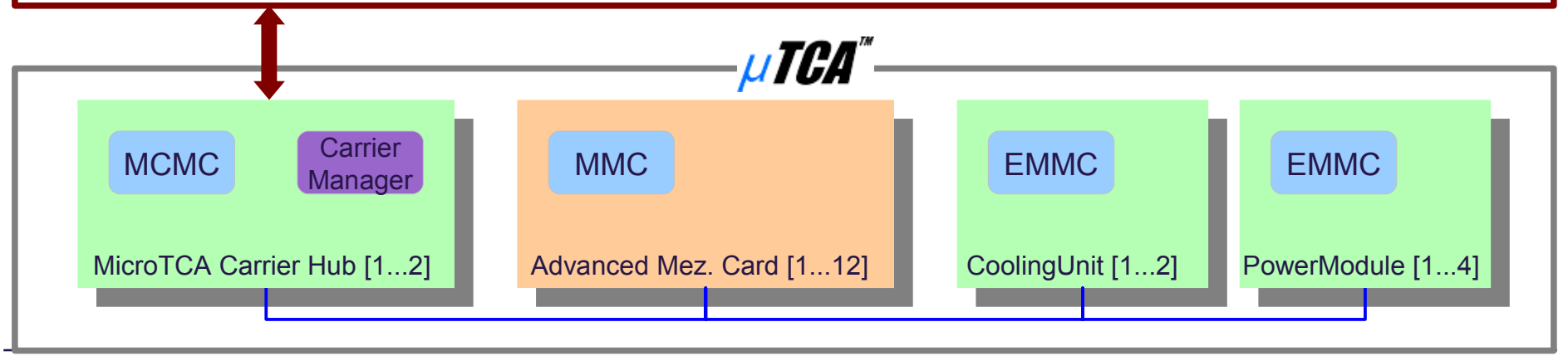
xTCA for Physics – Hardware Working Group



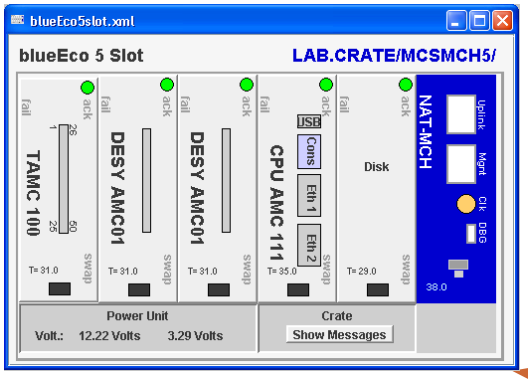
- µTCA rear transition modules – rear I/O for AMC
- Clock and trigger distribution (ATCA and µTCA)
  - Allow data Acquisition with ps stability
  - Guidelines for timing, synchronization and interlocks
- Define recommended AMC board sizes
- Specifications for ATCA RTM

Crate Management

- IPMI control system integration
  - Control System server for ATCA, µTCA and computers
  - IPMI communication via Ethernet to the crates
  - Extracts from IPMI the available information
  - Creates a dynamic list of AMC modules
  - Creates a dynamic list of sensors
  - Archives values and provides reset/boot commands to FPGAs or CPUs
  - Required configuration: one entry per crate (IP name)

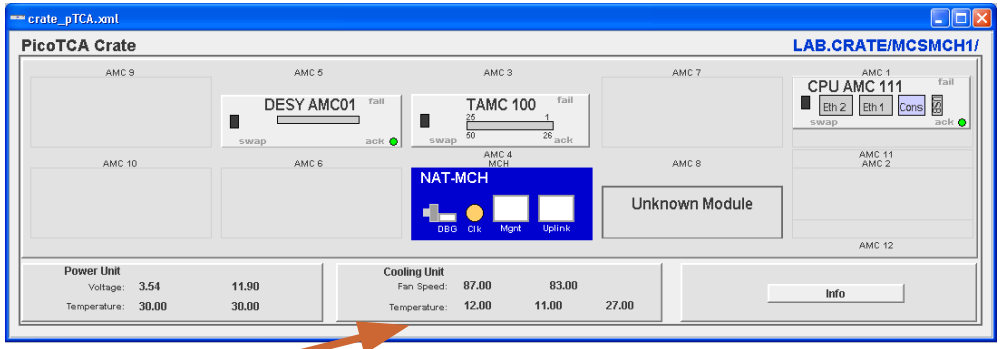


DOOCS Integration: Software Architecture



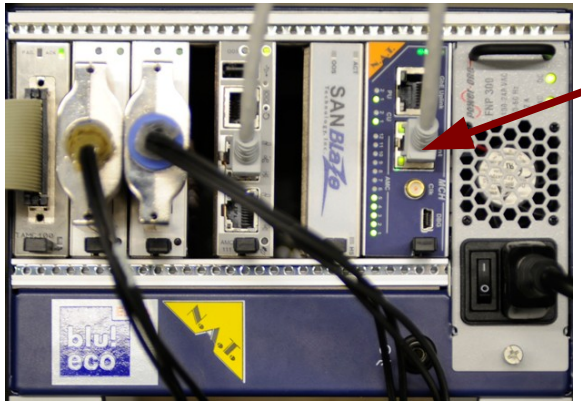
jddd

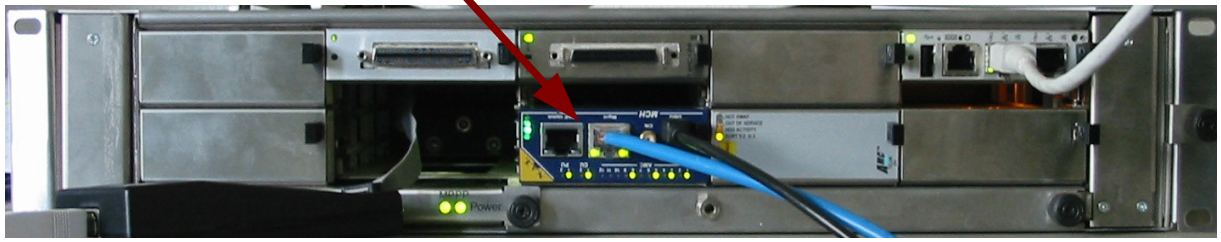
JAVA Application



DOOCS XTCA Crate Server
automatic configuration from IPMI

IPMI

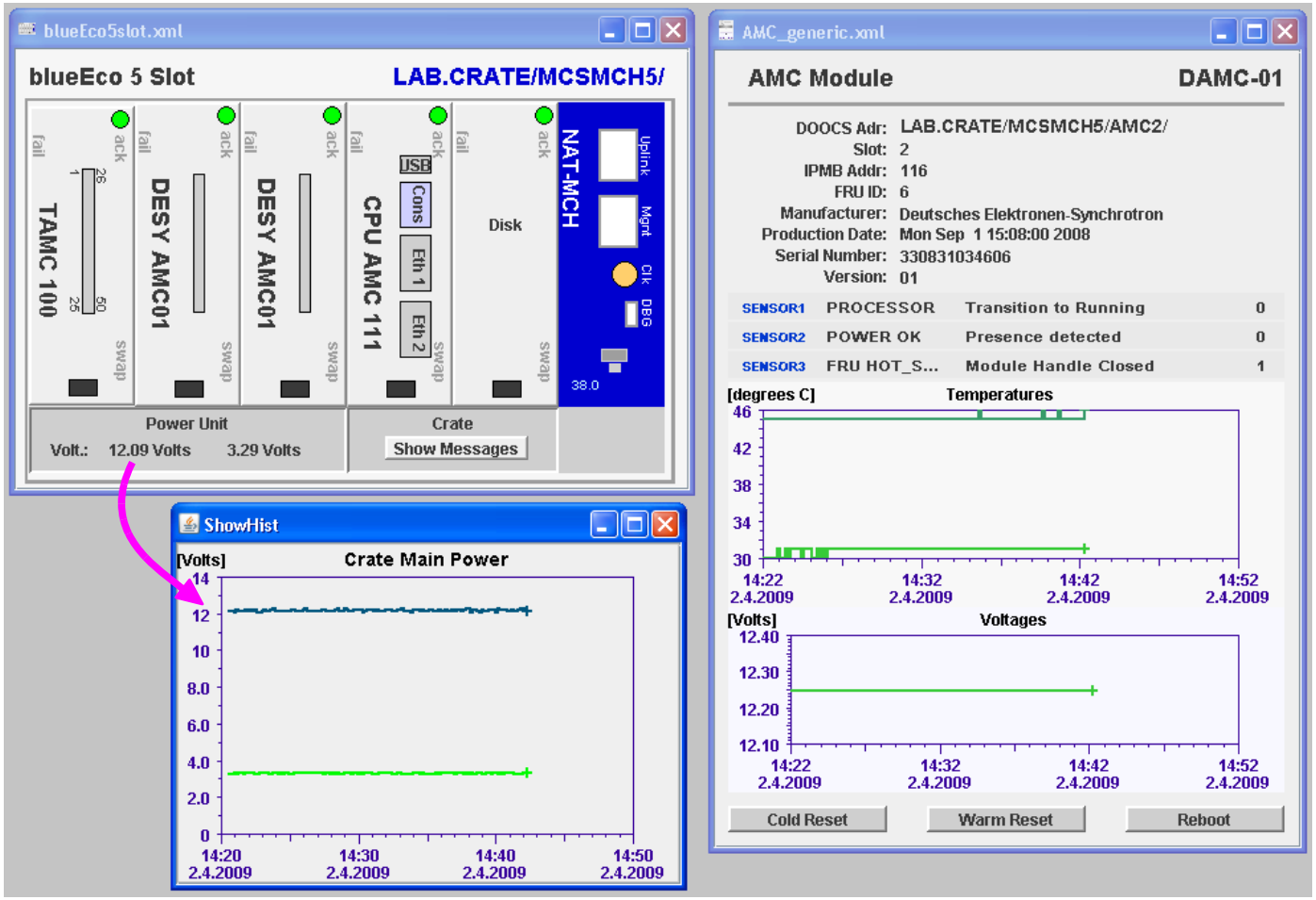




IPMI: Dynamic Crate View via DOOCS + jddd

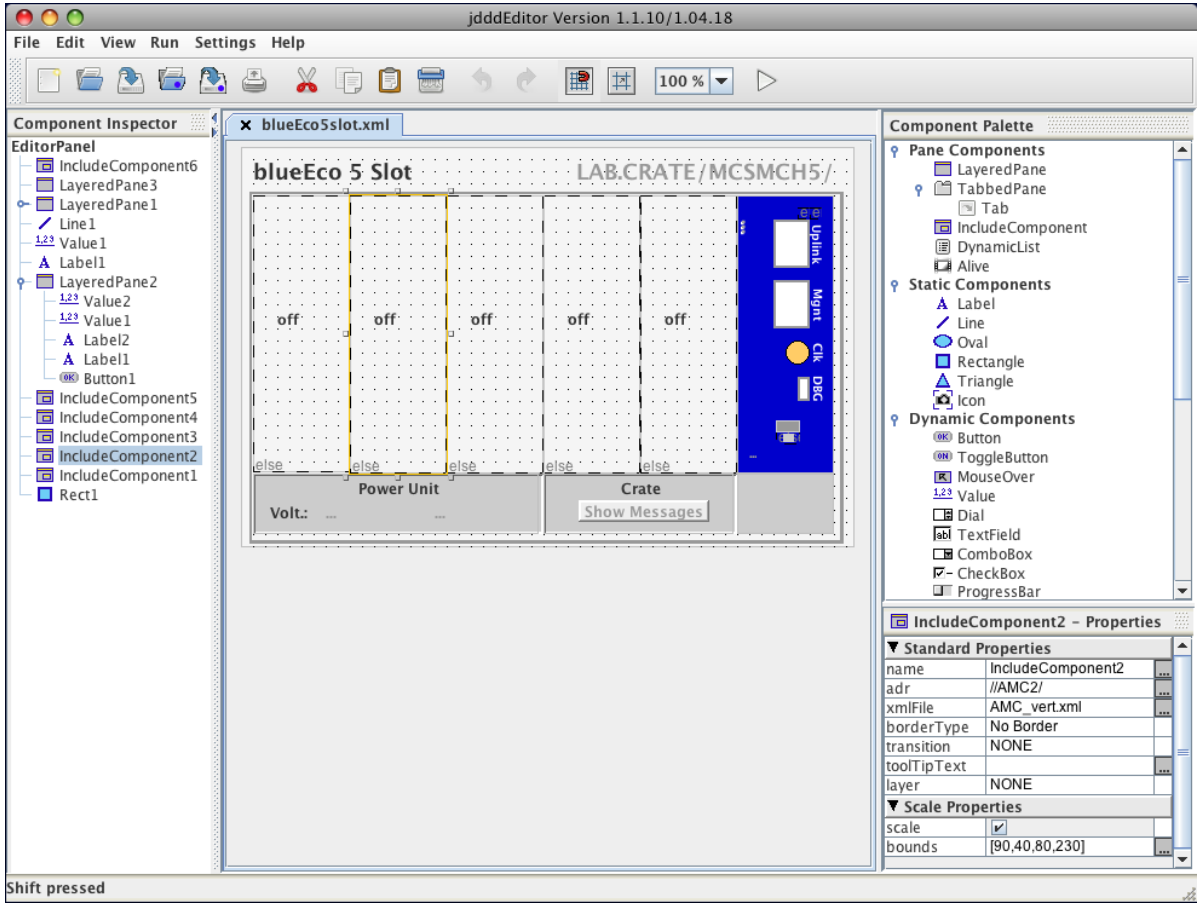
Panel shows actual inserted AMC modules and live status

- Click on a value shows a history plot
- Click on a AMC board displays details of the board
- The system is part of the accelerator control system
- The panels are designed by a graphical editor
- The std. AMC LEDs are indicating the real state



Created by a graphical editor 'jddd', one drawing per crate, one per AMC module

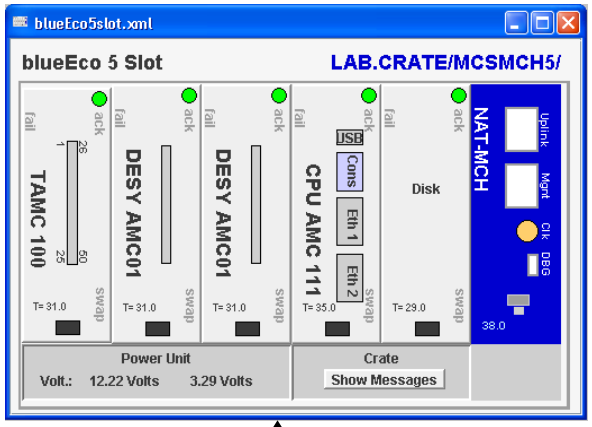
jddd: Java DOOCS Data Display



- Simple creation of complex control system panels
- Rich set of widgets for animated graphics and plots
- Hierarchical design with reusable components
- Has a plug-in interface to add other widgets
- Supports 4 control systems: has a data access layer

http://jddd.desy.de

jddd: Communication to 4 Control Systems



Address with name server translation:

FACILITY/DEVICE/LOCATION/PROPERTY

or direct:

doocs://host:libno/FAC/DEV/LOC/PROP

tine://Context/server/device/property

tango://host:port/domain/family/member/attr.

epics://ca_gw:ca_gw/channel_pv

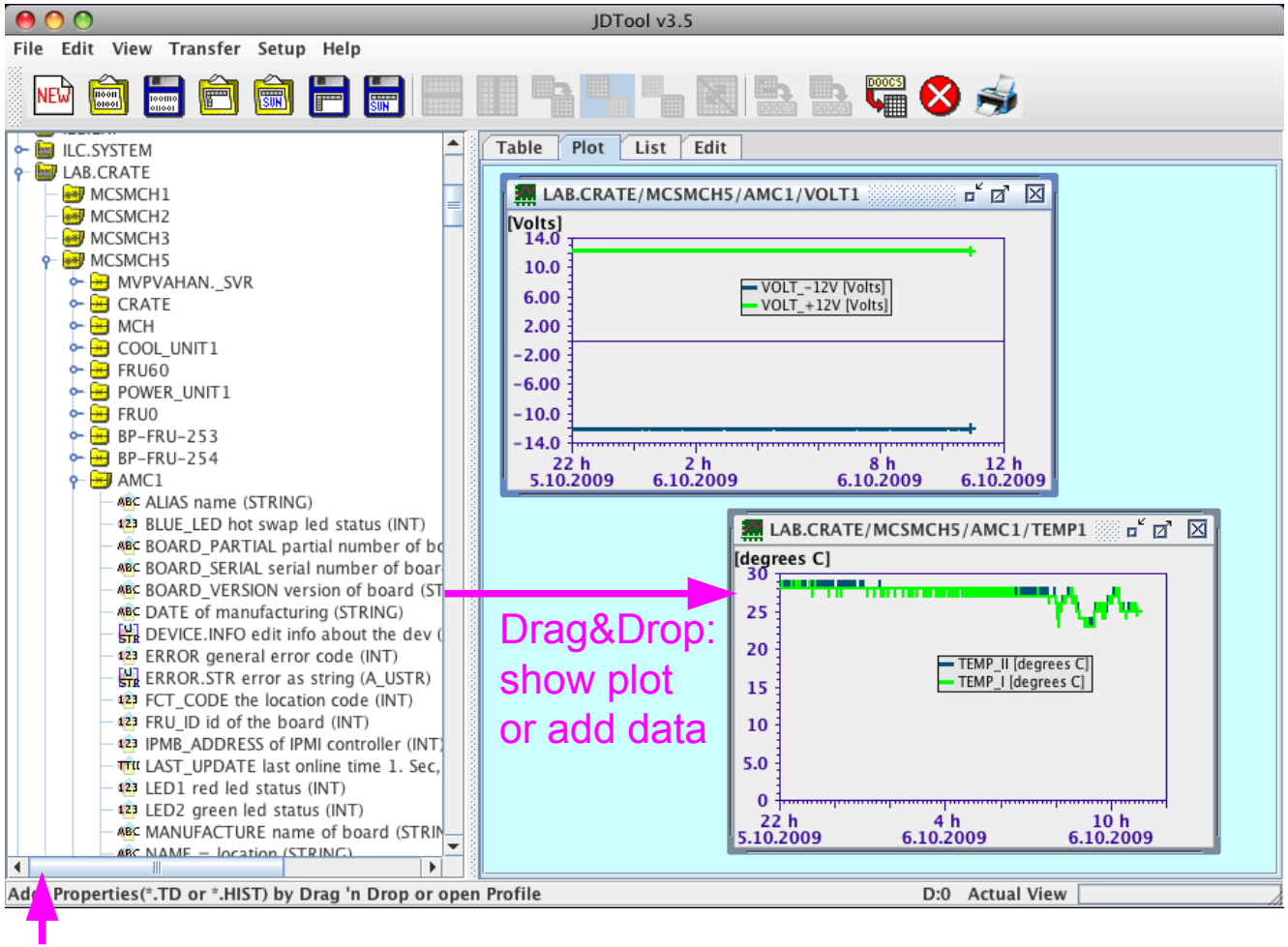
jdoocs.jar: wrapper to adapt the specifics

DOOCS TINE TANGO EPICS

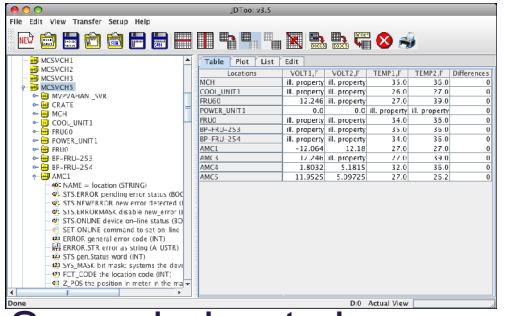
Name Server

Native protocol of the control system

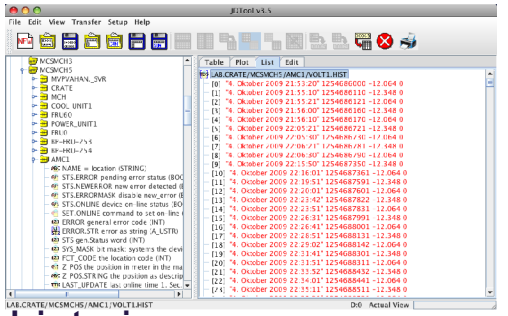
Generic Tool to Display all Values of the System



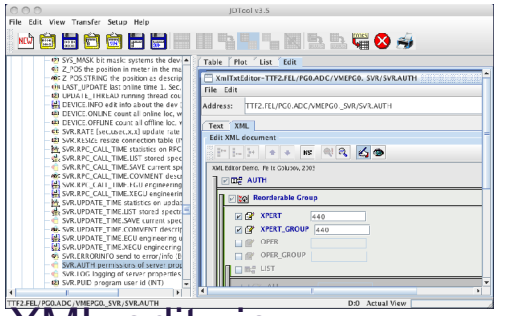
Hierarchical view of controls system addresses



Spread-sheet view

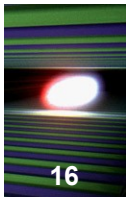


List view



XML edit view

Conclusions

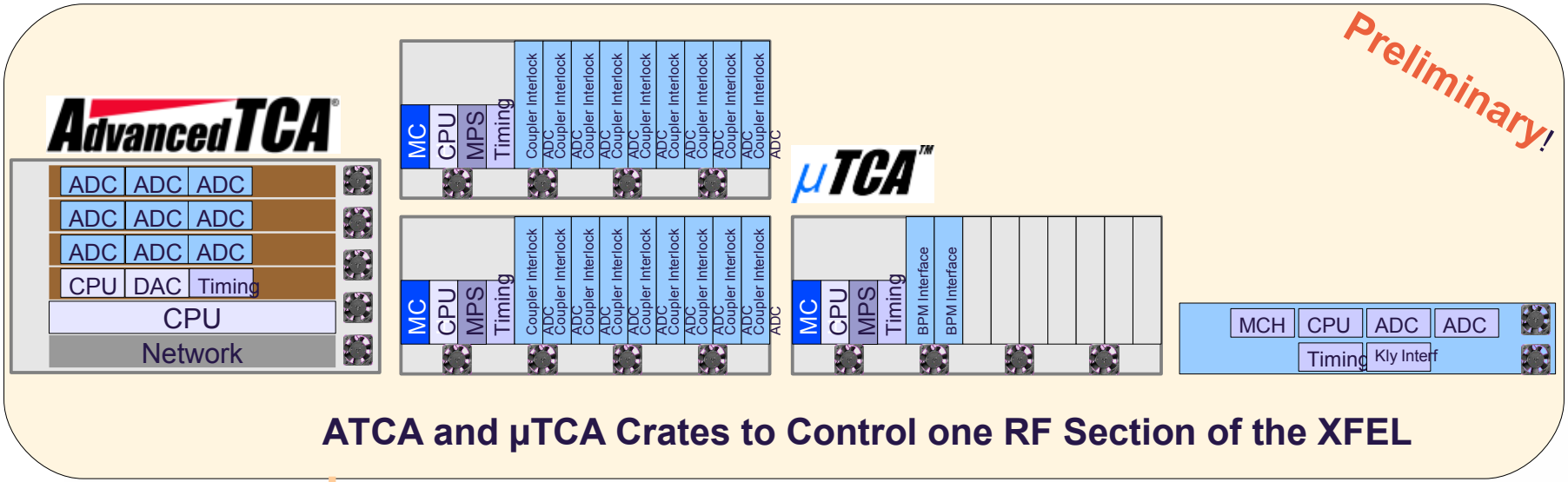


- Evaluation of xTCA:
  - Good, state-of-the-art technology
  - ATCA and µTCA covers a wide range of applications with one technology
- µTCA standard requires some add-ons:
  - PICMG working group “xTCA for Physics“
- Full Software integration of components in DOOCS:
  - IPMI, FPGA, driver and control system
- Crate management as part of the std. control system
- Development of new JAVA based generic applications
  - Jddd: editor for complex GUI panels
  - JDTool: general spread-sheet, table and plot tool

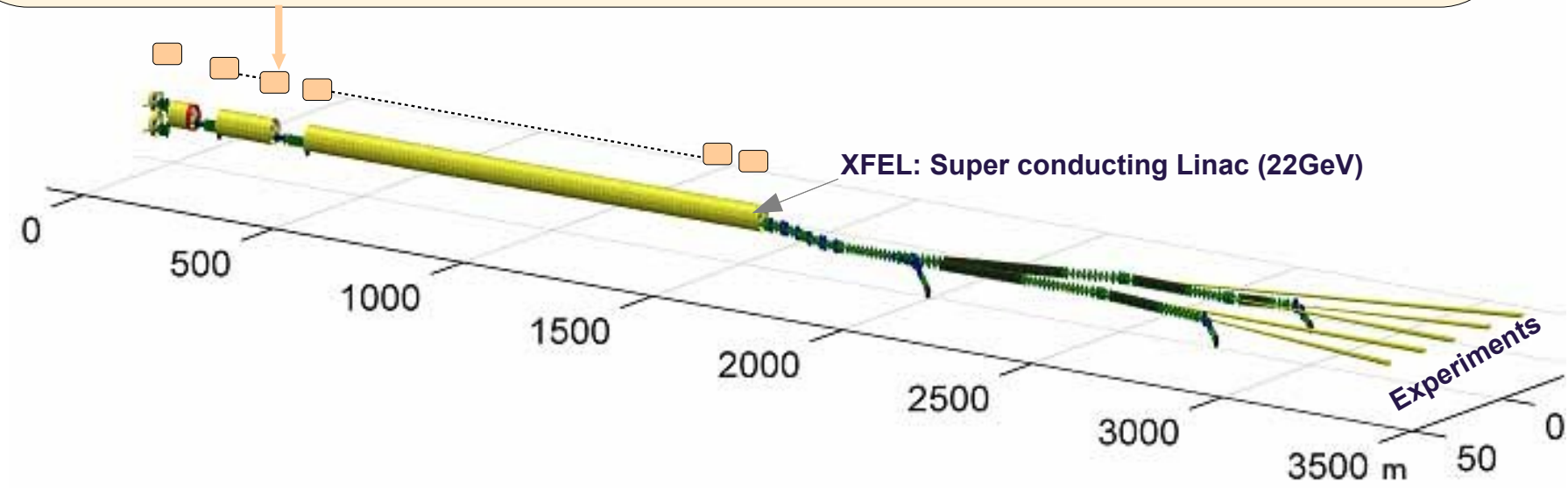
XFEL Status

backup

Geographical Layout of RF Stations



ATCA and µTCA Crates to Control one RF Section of the XFEL



Tested µTCA Crates